InP DHBT MMIC Power Amplifiers for Millimeter-Wave Applications

Squartecchia, Michele

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Technical University of Denmark

Michele Squartecchia

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PhD Thesis

DTU Electrical Engineering
Department of Electrical Engineering

MICHELE SQUARTECCHIA

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Supervisors:

Tom K. Johansen, Professor at the Electrical Engineering Department of DTU

Jean-Yves Dupuy, Research Department Head at III-V Lab

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This report was prepared by:
Michele Squartecchia

Advisors:
Tom K. Johansen, Professor at the Electrical Engineering Department of DTU
Jean-Yves Dupuy, Research Department Head at III-V Lab

DTU Electrical Engineering
Technical University of Denmark
Ørsted Plads, Building 348
2800 Kgs. Lyngby
Denmark

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ECTS:

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Preface

This thesis represents part of the outcome of the research conducted in the framework of the project "InP DHBT MMIC Technology for Millimeter-Wave Power Applications (IN-POWER)" funded by the European Commission under the Marie-Curie Action program FP7-PEOPLE-2013-ITN (project ID: 607647). The research work has been carried out in collaboration with the industrial partner III-V Lab, a joint research laboratory of Nokia-Bell Labs, Thales, and CEA Leti, located in Palaiseau (France), where all the circuits were fabricated and measured, and where I spent eighteen months during the PhD studies.

I would like to thank my supervisors Prof. Tom Johansen and Dr. Jean-Yves Dupuy for granting me the opportunity to pursue an exciting and challenging research topic and for their invaluable technical advices and friendly mentorship. I would also like to extend my gratitude to Agnieszka Konczykowska, Virginio Midili, Virginie Nodjiadjim, and Muriel Riet, who were directly involved in this project and played a crucial role with their expertise to the success of it. For his invaluable help in the measurement process, I have to thank Filipe Jorge.

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List of publications

During the PhD studies, the following papers have been published or accepted for publication:

1. M. Squartecchia, T. K. Johansen, J.-Y. Dupuy, V. Midili, V. Nodjiadjim, M. Riet, A. Konczykowska, "InP DHBT Ballasted Stacked-Transistor for Millimeter-Wave Power Amplifiers," *Proceedings of the Latin America Microwave Conference (LAMC)*, December 2018.

2. M. Squartecchia, T. K. Johansen, J.-Y. Dupuy, V. Nodjiadjim, V. Midili, M. Riet, A. Konczykowska, "E-Band InP DHBT MMIC Power Amplifier Based on Stacked Transistors," *Microwave and Optical Technology Letters*, (in press).

3. M. Squartecchia, T. K. Johansen, J.-Y. Dupuy, V. Midili, V. Nodjiadjim, M. Riet, A. Konczykowska, "Optimization of InP DHBT Stacked-Transistors for Millimeter-Wave Power Amplifiers," *International Journal of Microwave and Wireless Technologies*, August 2018.

4. M. Squartecchia, V. Midili, T. K. Johansen, J.-Y. Dupuy, V. Nodjiadjim, M. Riet, A. Konczykowska, "75 GHz InP DHBT Power Amplifier Based on Two-Stacked Transistors," *Proceedings of the Asia Pacific Microwave Conference (APMC),* November 2017.

5. M. Squartecchia, B. Cimoli, V. Midili, T. K. Johansen, V. Zhurbenko, "Design of a Planar Ultra-Wideband Four-Way Power Divider/Combiner Using Defected Ground Structures," *Proceedings of the 48^{th} European Microwave Conference (EuMC),* October 2017.

6. V. Midili, V. Nodjiadjim, T. K. Johansen, M. Squartecchia, M. Riet, J.-Y. Dupuy, A. Konczykowska, "InP DHBT technology for power amplifiers at mm-wave frequencies," *Microelectronics Journal*, vol. 67, pp. 111-119, August 2017.

7. V. Midili, V. Nodjiadjim, T. K. Johansen, M. Squartecchia, M. Riet, J.-Y. Dupuy, A. Konczykowska, "3D thermal simulations and modeling of multi-finger InP DHBTs for millimeter-wave power amplifiers," *Proceedings of the SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC)*, 2017.

8. V. Zhurbenko, T. K. Johansen, M. Squartecchia, V. Midili, O. Rybalko, M. Riet, J.-Y. Dupuy, V. Nodjiadjim, A. Konczykowska, "Low Conversion Loss 94 GHz and 188 GHz Doublers in InP DHBT Technology," *Proceedings of the International Workshop on Integrated Nonlinear Microwave and Millimetrewave Circuits (InMMiC),* 2017.

9. T. K. Johansen, V. Midili, M. Squartecchia, V. Zhurbenko, V. Nodjiadjim, J.-Y. Dupuy, M. Riet, A. Konczykowska, "Large-signal Modeling of Multi-finger InP DHBT Devices at Millimeter-wave Frequencies," *Proceedings of the International Workshop on Integrated Nonlinear Microwave and Millimetrewave Circuits (InMMiC),* 2017.

10. V. Midili, M. Squartecchia, T. K. Johansen, V. Nodjiadjim, M. Riet, J.-Y. Dupuy, A. Konczykowska, "A Physical Based Equivalent Circuit Modeling Approach for Ballasted InP DHBT Multi-finger Devices at Millimeter-wave Frequencies," *Proceedings of the IEEE Compound Semiconductor Week*, 2016.

11. M. Squartecchia, T. K. Johansen, V. Midili, "Design Procedure for Millimeter-wave InP DHBT Stacked Power Amplifiers," *Proceedings of the International Workshop on Integrated Nonlinear Microwave and Millimetrewave Circuits (InMMiC),* 2015.

12. R. S. Michaelsen, T. K. Johansen, K. Tamborg, M. Squartecchia, "Flicker Noise Comparison of Direct Conversion Mixers Using Schottky and HBT Dioderings in SiGe:C BiCMOS Technology," *Proceedings of the International Workshop on Integrated Nonlinear Microwave and Millimetrewave Circuits (InMMiC),* 2015.

13. V. Midili, V. Nodjiadjim, T. K. Johansen, M. Riet, J.-Y. Dupuy, A. Konczykowska, M. Squartecchia, "Electrical and Thermal Characterization of Single and Multi-finger InP DHBTs," *Proceedings of the 10^{th} European Microwave Integrated Circuits Conference (EuMIC),* 2015.

14. M. Squartecchia, T. K. Johansen, R. S. Michaelsen, "Design of a SiGe BiCMOS Canceller for Low Frequency Noise Reduction in Direct Conversion Receivers," *Proceedings of the 1^{st} URSI Atlantic Radio Science Conference,* 2015.

Abstract

This thesis reports on the analysis, design and implementation of E-band (71-86 GHz) power amplifiers in InP double heterojunction bipolar transistors (DHBTs) technology intended for next generation wireless communications systems. The wireless communication context and the typical requirements of power amplifiers are briefly discussed, pointing out the main limitations arising at such high frequencies. To extend the power capabilities of the InP DHBT technology, the possibility of applying the stacked-transistor concept has been investigated in detail. A theoretical analysis based on the interstage matching between all the single transistors has been developed starting from the small-signal equivalent circuit. The analysis has been extended by including large-signal effects and layout-related limitations, which are thoroughly characterized by electromagnetic (EM) simulations. An evaluation of the maximum number of stacked transistors for positive incremental power and gain is also carried out. To validate the analysis, two-, three-, and four-stacked matched power cells have been realized as monolithic microwave integrated ciruits (MMICs) and tested for E-band operation. For instance, at 81 GHz, the two-stacked transistor power cell exhibits a small-signal gain of 6.4 dB, a measured maximum output power of 14.3 dBm and a peak power added efficiency (PAE) of 4.2 %. For the three-stacked transistor, a small-signal gain of 8.3 dB, a saturated output power of 15 dBm and a PAE of 5.2 % have been obtained at 81 GHz. At the same frequency, the four-stacked transistor achieves a small-signal gain of 11.5 dB, a saturated output power of 14.9 dBm and a peak PAE of 3.8 %.

Various power amplifiers featuring parallel power combining have been designed as well. Good results are obtained from a four-way combined three-stacked configuration and from a two-stage eight-way combined power amplifier, which achieves an output power higher than 21.4 dBm at 75 GHz.

The InP technology employed in this project is developed at III-V Lab (France) in two different processes. One is suited for high-speed mixed-signal applications and is denoted as SHARC process. The other, intended for power amplifiers, is denoted as SAND process. During the course of the project, III-V Lab's clean rooms have been relocated in new premises in Palaiseau, leading to delays and difficulties in wafer fabrication. Albeit all circuits have been designed with SAND models, the functional fabricated wafers were in SHARC. Back-simulations, however, corroborated simulations and experimental results.

List of Acronyms

4G	Fourth Generation of cellular mobile communications
5G	Fifth Generation of cellular mobile communications
ADS	Advanced Design System (software tool from Keysight)
ASK	Amplitude Shift Keying
BEOL	Back-End-of-Line
BER	Bit Error Ratio
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BV	Breakdown Voltage
CPW	Coplanar Waveguide
DC	Direct Current
DHBT	Double Heterojunction Bipolar Transistor
DUT	Device Under Test
ECPW	Elevated Coplanar Waveguide
EHF	Extremely High Frequencies
EM	Electromagnetic
FET	Field Effect Transistor
FSPL	Free Space Path Loss
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSG	Ground-Signal-Ground
GSMBE	Gas Source Molecular Beam Epitaxy
HBT	Heterojunction Bipolar Transistor
HDTV	High Definition Television
HEMT	High Electron Mobility Transistor
InGaAs	Indium Gallium Arsenide
InP	Indium Phosphide
ISM	Industrial, Scientific and Medical
JFOM	Johnson Figure-of-Merit
LNA	Low-Noise Amplifier
LOS	Line-of-Sight
MAG	Maximum Available Gain
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
MPA	Medium Power Amplifier

MSG	Maximum Stable Gain
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
SDD	Symbolically Defined Device
SiGe	Silicon Germanium
SOA	Safe Operating Area
SOI	Silicon on Insulator
TFML	Thin Film Microstrip Line
TFR	Thin Film Resistor
UCSD	University of California San Diego (a particular transistor model)
VNA	Vector Network Analyzer

CHAPTER 1

Introduction

1.1 Millimeter-wave Characteristics

Millimeter-waves (mm-waves) represent the portion of the electromagnetic spectrum featuring wavelengths ranging from 1 mm to 10 mm, corresponding to the frequency range in the free space spanning from 30 GHz to 300 GHz, also known as extremely high frequencies (EHF). While previously reserved for military and scientific domains, mm-waves have been attracting great interest in academia and industry during the last decades and are now available also for commercial use. The primary reason to explore such high frequencies is the availability of large bandwidths to extend the capacity of currently congested wireless networks. Another motivation is the possibility to leverage the short wavelengths and achieve high antenna gain and high resolution in imaging and sensing applications. This trend is made possible thanks to the great advancements in semiconductor technology, where new devices with small feature size allow unprecedented frequencies of operation in electronic systems.

Electromagnetic waves experience a power fall-off proportional to the square of the distance R from the emitting source and inversely proportional to the square of the wavelength λ. This attenuation is usually expressed in dB by means of the free-space-path-loss (FSPL) as [1]:

$$FSPL = 10\log_{10}\left(\frac{4\pi R}{\lambda}\right)^2. \tag{1.1}$$

This relationship could seem a big limitation for mm-waves, as it clearly states that a strong attenuation occurs as the frequency increases. However, an advantage of mm-waves is that, given an antenna size, the radiated power can be concentrated in a narrower beam thanks to the shorter wavelengths so that gain and directivity can be increased significantly to overcome these losses. Advanced antenna arrays can also be used to form pencil-like beams to establish reliable connections in point-to-point links ensuring low interference and security against interceptions. An important limitation for mm-waves is associated to the mechanisms of absorption in the atmosphere, which cause a power attenuation somehow proportional to the frequency, but with peaks and valleys depending on the molecular resonance characteristics of oxygen and water vapor [2, 3]. As shown in Figure 1.1, there are some frequency ranges exhibiting low attenuation (commonly referred to as atmospheric windows) such as the W-band (75-110 GHz) which are well suited for wireless

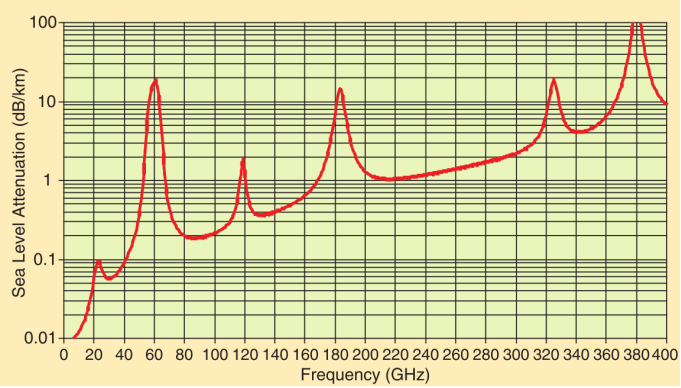


Figure 1.1: Atmospheric attenuation at sea level as a function of frequency [3].

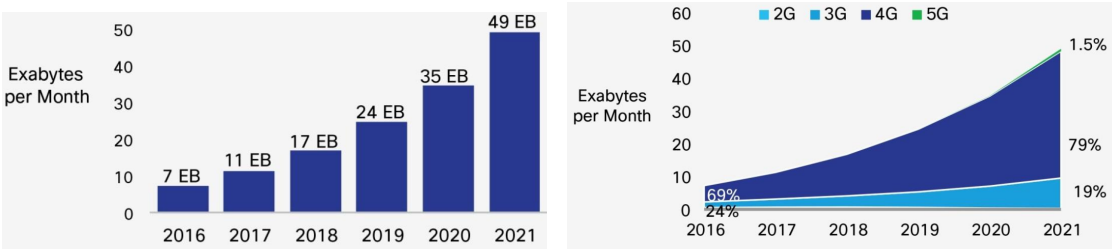
communications and radar applications even at long distances. Other frequency ranges, such as that around 60 GHz, are characterized by peak levels of attenuation, but many applications exploit this feature in the realization of short range and indoor wireless networks. Additionally, rain and humidity can impair the performance of a mm-wave signal traveling in open air and physical objects can block its propagation. As a consequence, line-of-sight (LOS) connectivity is often required at mm-wave frequencies.

1.1.1 Applications

The most important use for mm-waves is the wireless transmission of huge amount of data at high speed and low latency. Within this kind of applications, a distinction can be made depending on the range of operation: 1) long range wireless transmissions, which include HDTV broadcasting, backhaul radio links at E-band (71-76 GHz and 81-86 GHz) or satellite communications; 2) short range wireless communications taking place in the unlicensed industrial-scientific-medical (ISM) range between 57 and 64 GHz with the standardized WirelessHD; 3) close-proximity wireless communications which are envisioned to take place even at higher frequencies such as the D-band (110-170 GHz) for data transfer between consumer appliances or even in PCB-to-PCB (printed circuit board) and chip-to-chip wireless connections [4].

Millimeter-wave radars have been widely used for military applications, but are now widespread also in commercial automotive systems such as collision avoidance and obstacle detection. The frequency band reserved for these applications is between 76 and 81 GHz and allow very high resolution and precise movements detection. They are often realized as system-on-chip with high integration technologies.

Human body scanners are becoming popular in airports security systems. With a low transmit power and a frequency range around 94 GHz, they are able to detect dangerous objects and cause no harm for the human body. Low intensity mm-waves have been proved also beneficial in medical applications such as pain treatment between 40 and 70 GHz [5].



(a) (b)

Figure 1.2: Mobile data traffic forecasts by Cisco [9]

1.2 E-band Communication Systems

The E-band is favorable for high-rate and long-range wireless communications due to the small atmospheric attenuation (only about 0.5 dB/km). With a total frequency allocation of 10 GHz (71–76 GHz and 81–86 GHz) it allows data speeds up to 10 Gbps in full duplex configuration envisioned for backhaul cellular networks, broadband Internet access and satellite communications [6, 7, 8]. Backhaul links are often realized in optical fibers, but in certain situation this solution can result unfeasible or economically inconvenient and the wireless counterpart represents a viable alternative. However, attaining comparable data-rates is a big challenge. Until not long ago, the radio interface between base stations and users' handsets was the bottleneck for high speed communications. With the recent advancements of mobile technologies and the increasing number of users, the data throughput in backhaul networks is growing exponentially. As predicted by the recent Cisco forecasts on mobile data traffic [9], the total demand will reach volumes as high as 49 Exabytes per month in a few years (Figure 1.2(a)). While the fourth generation (4G) infrastructure will still be the mainstream (Figure 1.2(b)), new technologies and standards are being developed in the framework of the upcoming fifth generation (5G), which certainly will heavily rely on mm-wave frequencies. In order to accommodate such data explosion, backhaul networks should be scaled accordingly by increasing the number of connections and improving channel capacity. Complex modulation techniques have been developed recently to increase the spectral efficiency, but enlarging the available bandwidths represent the ultimate solution for high speed and high throughput.

Figure 1.3 shows a conceptual diagram with essential components making up a modern wireless communication front-end employing a complex modulation format such as quadrature amplitude modulation (QAM), where the in-phase and quadrature baseband signals are denoted by $I(t)$ and $Q(t)$, respectively. The design always starts with the evaluation of the link-budget, which imposes a minimum value for the received power in order to achieve robustness and low error rates. In a point-to-point radio link it can be expressed as [10]:

$$P_{\mathrm{Rx}} = P_{\mathrm{Tx}} + G_{\mathrm{A,Tx}} + G_{\mathrm{A,Rx}} - FSPL - L_{\mathrm{atm}}\,(\mathrm{dBm}). \tag{1.2}$$

It states that the power P_{Rx} at the receiver front-end is proportional to the transmitted power P_{Tx} and the antenna gain of both the transmitter and receiver $G_{\mathrm{A,Tx}}$ and $G_{\mathrm{A,Rx}}$, respectively. It is inversely proportional to the free-space-path-loss $FSPL$ and to the atmospheric attenuation

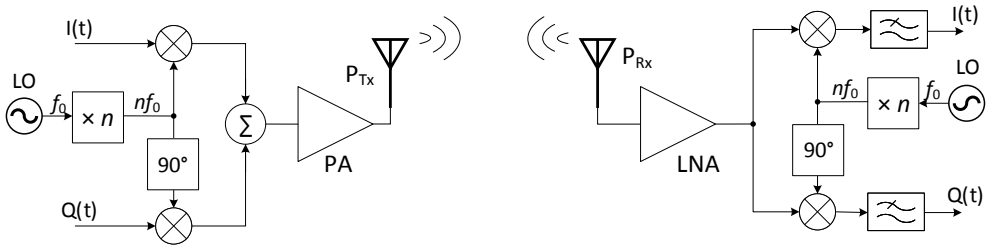


Figure 1.3: Conceptual diagram of a modern point-to-point wireless communication system.

L_{atm}. Depending on the required error rate and the particular modulation format, a lower limit is often imposed on the value of P_{Rx}, which in any case should be higher than the noise floor. As mentioned earlier, antenna gain can be improved as frequency increases so that the effects of $FSPL$ are partially counterbalanced. Atmospheric windows can be selected to alleviate the effects of L_{atm}, and this is why the E-band has been selected for relatively long range communications. What remains is P_{Tx} optimization, which is perhaps the biggest challenge in mm-wave wireless communications as this parameter usually tends to decrease considerably with the increasing frequency. The ultimate system component delivering transmit power to the transmit antenna is the power amplifier (PA), whose task is to boost the strength of the modulated signal and whose design is one of the most critical part in mm-wave wireless communication systems. To have an idea of the order of magnitude of the transmitted power required in a practical application, an example is reported in [27]: a 1-km point-to-point E-band radio link with a 64-QAM modulation format, an antenna gain of 50 dBi, a receiver sensitivity of -40 dBm and a specified bit error rate (BER) of 10^{-6} require a transmitted power of approximately 20 dBm. In the receiver front-end, the signal detected by the antenna is amplified by the low-noise amplifier (LNA) before being demodulated and reconstructed by the baseband signal processing systems.

1.3 E-band Power Amplifiers

Power amplifiers are needed to increase the power level of the modulated signal to be transmitted, so as to make P_{Tx} comply with the requirements of the link-budget. Nowadays, E-band power amplifiers are usually implemented in monolithic microwave (or mm-wave) integrated circuit (MMIC) technologies, leveraging the great advancements in semiconductor fabrication processes, which have allowed recently to achieve high frequency and high power densities. There are several key performance metrics characterizing power amplifiers. Optimizing all of them at the same time is often unfeasible and trade-offs have to be taken, favoring one parameter or the other depending on the particular application and specifications. Some of the most important performance parameters of power amplifiers are recalled here, emphasizing the context of E-band wireless communications.

1.3.1 Gain

There are several definitions of power gain and the most important ones for amplifier characterization are [12]:

- the *operating power gain*, defined as the ratio of the power delivered to the output load P_{out} to the input power P_{in} entering the amplifier itself:

$$G_P = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}}; \tag{1.3}$$

- the *available power gain*, defined as the ratio of the available power at the output of the amplifier $P_{\mathrm{Av,a}}$ to the power available from the source $P_{\mathrm{Av,s}}$:

$$G_A = \frac{P_{\mathrm{Av,a}}}{P_{\mathrm{Av,s}}}; \tag{1.4}$$

- the *transducer power gain*, defined as the ratio of the power delivered to the output load P_{out} to the power available from the source $P_{\mathrm{Av,s}}$:

$$G_T = \frac{P_{\mathrm{out}}}{P_{\mathrm{Av,s}}}. \tag{1.5}$$

The transducer power gain is the most widely used in power amplifier characterization as it represents the power "added" to the output load by the presence of the power amplifier compared to the situation where only the source is present. The transducer power gain definition takes into account all the mismatches at the input and output, while the operating power gain G_P or the available power gain G_A depends only on the output or source load, respectively. In this work, unless otherwise stated, we characterize power amplifiers with the transducer power gain and indicate it as G for simplicity.

Being the amplifier a nonlinear element, gain is not constant: at low input power levels it corresponds to the linear gain; as the power level increases beyond a certain value the gain starts to drop and eventually reaches zero. This behavior is referred to as gain compression.

At mm-waves, with the transistors operating at frequencies of the same order of magnitude as the cut-off f_T or the maximum frequency of oscillation $f_{\max}$, gain optimization is extremely important and is often pursued by cascading two or more amplifier stages. Moreover, to maintain acceptable levels of gain, Class A or light Class AB bias has to be chosen, so as to ensure also linear operation over a wide dynamic range. On the other hand, a disadvantage of Class A biasing is a rather poor efficiency [13].

1.3.2 Output Power

The power delivered to the output load by a power amplifier at a given frequency is defined as:

$$P_{\mathrm{out}} = \frac{1}{2}\Re[V_{\mathrm{out}} \cdot I^*_{\mathrm{out}}], \tag{1.6}$$

where V_{out} and I_{out} indicate the output voltage and current amplitudes at the specified frequency. This relation indicates that in order to optimize and increase the transmitted power, the output

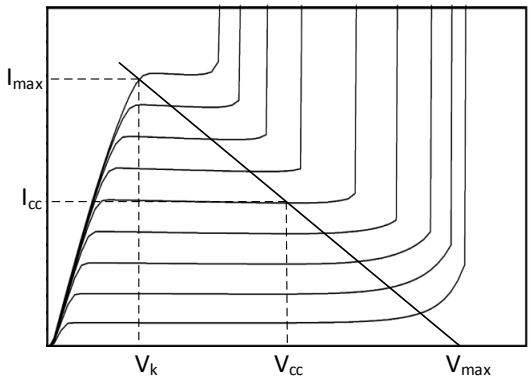


Figure 1.4: Load line principle for the determination of the optimum load impedance of a power amplifier in Class A bias condition.

voltage $V_{\rm out}$ and current $I_{\rm out}$ of an amplifier must be optimized. In all practical devices, the upper limit for $V_{\rm out}$ is set by the breakdown voltage BV established by the maximum electric field which can be sustained without incurring failure. As the current is also constrained within a maximum value depending on thermal issues and gain degradation, it follows that the output power is limited. More importantly, in all semiconductors there is an inverse proportionality between these values and the frequency of operation, as demonstrated by Johnson in [14]. It follows that the power capabilities of a particular device follow the well known power-frequency squared relationship [15]:

$$P_{\rm out} \cdot f^2 = const., \tag{1.7}$$

which represents a clear limitation for power amplifiers operating at mm-wave frequencies. To extract the highest possible power from a device, a particular value of the load impedance has to be chosen in such a way that both $V_{\rm out}$ and $I_{\rm out}$ experience maximum swing. This is determined by the load line approach shown in Figure 1.4. The output characteristics of a transistor, including breakdown mechanisms, are shown together with the optimum load line in Class A bias condition, for which $I_{\rm cc} = I_{\rm max}/2$ and $V_{\rm cc} = (V_{\rm max} + V_{\rm k})/2$, where $V_{\rm k}$ is the knee voltage. The optimum value of the load resistance maximizing the output power is given by:

$$R_{\rm opt} = \frac{(V_{\rm max} - V_{\rm k})}{I_{\rm max}}, \tag{1.8}$$

and the corresponding output power is:

$$P_{\rm opt} = \frac{1}{8} I_{\rm max} (V_{\rm max} - V_{\rm k}). \tag{1.9}$$

In practice, the optimum load is actually a complex one and its determination is carried out by means of load-pull measurements performed on the device properly biased [13]. In general, the found value of the optimum load differs from the complex conjugate matching which would optimize the gain.

1.3.3 Linearity

In modern wireless communications, power amplifier linearity is one of the most important parameters. Nonlinearities usually lead to reduced dynamic ranges because of gain compression and to the generation of spurious frequencies and intermodulation distortion. This can be a serious problem in wireless transmitters, especially in nonconstant envelope modulations, such as amplitude shift keying (ASK) and higher order QAM methods, because the information content could result altered. Moreover, in multicarrier systems such as orthogonal frequency division multiplexing (OFDM), spurious signals may appear in adjacent channels and interfere with other communication links. The easiest and most natural approach to avoid as much as possible nonlinearities is a proper selection of the bias point so as to ensure that voltage and current swings remain as long as possible in the linear region. Class A operation is the best option to maintain high linearity. However, reducing the conduction angle not always results in much worse performances in terms of linearity [13], but the disadvantage would be a reduced gain, which is a precious parameter to preserve at mm-waves.

Advanced techniques have been developed to reduce the detrimental effects of nonlinearities, such as feedback, feedforward and digital predistorion. These techniques are extremely difficult to apply at mm-waves and represent a hot reasearch topic.

1.3.4 Efficiency

Essentially, what a power amplifier does is converting DC power to RF power according to the stimulus received at the input represented by the input signal to be amplified. How good is the power amplifier at accomplishing this task is measured by the efficiency. There are several definitions of efficiency for a power amplfier. The simple ratio between the output RF power and the DC power is the collector efficiency (or drain efficiency in case the amplifier is implemented on FET transistors):

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{DC}}} \tag{1.10}$$

which is usually measured in percentage. Assuming a Class A operation and neglecting the knee voltage V_{k}, $P_{\mathrm{DC}} = V_{\max} I_{\max}/4$, and using equation (1.7), it can be found that the theoretical collector efficiency is 50 %. Practically, and especially in sub-micrometer integrated devices, V_{k} can be a significant percentage of the bias voltage V_{cc}, so the theoretical 50 % is quite optimistic. The efficiency can be considerably increased with other classes of operation and can reach theoretical values of 100 % in switchmode power amplifiers.

A more meaningful and useful definition of efficiency is the *power-added efficieny* which takes into account also the power contribution of the input RF signal:

$$PAE = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{DC}}} = \eta \left(1 - \frac{1}{G}\right). \tag{1.11}$$

It is generally observed that PAE decreases rapidly with frequency as a consequence of power and gain degradation. Conversely, PAE increases with input power up to a peak value which is reached when the amplifier is strongly saturated.

1.4 Semiconductor Technologies

Great advancements have been achieved during the last few decades in semiconductor device technology. High resolution photolithography and new sophisticated techniques for layer deposition have permitted cost-effective fabrication of highly down-scaled transistors featuring cut-off frequencies up to the terahertz region [17]. Several technologies exist which are suitable for power applications [18]. The choice of one over the other is based on the particular application and performance specifications, such as power capabilities, maximum frequency of operation, thermal conductivity, reliability, costs. First of all, material properties constitute the primary factor determining the performance of a particular device. The physical parameters of interest for mm-wave applications are the electron and hole mobilities μ_n and μ_p, which determine, together with the saturation velocity $v_{\rm sat}$, the carrier transport properties. The intrinsic breakdown field E_B and the thermal conductivity K are also important for power applications. To evaluate and compare different semiconductor materials, some figures of merit have been devised. The most widely used to assess power capabilities is the Johnson figure-of-merit [14, 19]:

$$JFOM = \frac{E_B v_{\rm sat}}{2\pi}. \tag{1.12}$$

At high frequencies, compound semiconductor materials are often preferred for their better carrier transport characteristics and isolating substrates, which allow the realization of high-Q passive components. To further enhance the performances, heterojunction structures and advanced techniques of band-gap engineering are used to design high performance devices such as heterojunction bipolar transistors (HBTs) and high electron mobility transistors (HEMTs). Gallium arsenide (GaAs) is one of the earliest technologies having been developed for MMIC power amplifiers and currently exhibits moderate power capabilities up to the W-band [20, 21]. Silicon-based technologies have been usually relegated to low frequency applications, but recently silicon germanium (SiGe) HBTs have been introduced in BiCMOS environments having high levels of integration. Research efforts in this context have been deployed to overcome the limited breakdown voltage, and power amplifiers with good performances have been demonstrated up to 120 GHz [22]-[24]. Even the traditional CMOS process is finding application for power amplification at mm-waves and the silicon-on-insulator (SOI) process has been developed to alleviate substrate losses [25]-[27].

Recent breakthroughs in mm-wave power amplifiers are represented by the recent advent of gallium nitride (GaN) and indium phosphide (InP) technologies, the former having the highest JFOM. MMIC power amplifiers implemented on GaN have been demonstrated exhibiting output power levels higher than 30 dBm up to 96 GHz [28, 29]. On the other hand, InP devices are the fastest transistors. Due to the significant downscaling of the features size, both InP HEMTs and HBTs have demonstrated $f_{\rm max}$ values exceeding 1 THz [30]. Double heterojunction bipolar transistors (DHBTs) exhibit even superior performance owing to the wide bandgap InP collector and higher power densities. Thermal effects, however, can degrade the overall capabilities and some research groups are investigating the possibilities of using heat spreader layers such as diamond [36].

A survey and comparison of the most significant results on mm-wave power amplifiers reported during the last few years can give an explanatory picture of the different capabilities and progress of

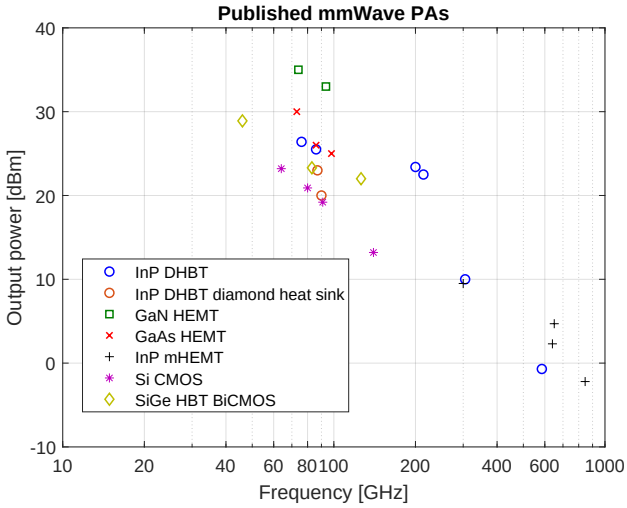


Figure 1.5: State of the art of millimeter-wave power amplifiers for different technologies recently published [20]-[38].

the main technologies. Such a comparison is shown in Figure 1.5, where the output power obtained at MMIC level are reported.

1.5 Thesis Overview

This work describes the analysis and design of E-band power amplifiers implemented in InP DHBT technology realized at III-V Lab, France.

In **Chapter 2**, the InP DHBT technology used in this project will be described. The main features of the active devices are reported for the two different processes available at III-V Lab. One process is optimized for high-speed mixed-signal applications and is denoted as "SHARC" process; the other one is optimized for power applications and is denoted as "SAND" process. Single- and multi-finger devices will be described and some details on their modeling will be given. Ballasted devices will be also introduced. A description of the back-end-of-line (BEOL) and the design kit of this technology follows.

In **Chapter 3**, the analysis and design of the basic power cells are reported. The main focus here is the invesetigation of the applicability of the stacked-transistor topology to InP DHBT technology and the existing limitations of this approach will be discussed. The analysis is first based on the small-signal model of transistors and is then extended to large-signal model and layout optimization.

The analysis conducted in **Chapter 3** is validated by experimental results reported in **Chapter 4**, where matched MMIC power cells are described together with measurements.

Some of the power cells described in **Chapter 3** are used as building blocks and combined together for the implementation of larger MMIC power amplifiers. These circuits are presented in **Chapter 5**. To enhance the output power, four- and eight-way parallel power combining techniques are employed and, to improve the gain, two-stage MMIC power amplifiers are designed.

Although all the designs have been optimized using SAND transistor models, the MMIC circuits have been realized and measured on the SHARC process. To validate the design approach, back-simulations have been carried out on SHARC models. SHARC and SAND simulations have been compared to better evaluate the performance differences between the two processes.

A brief discussion on the obtained results and an outlook to perspective works are given in the concluding **Chapter 6**.

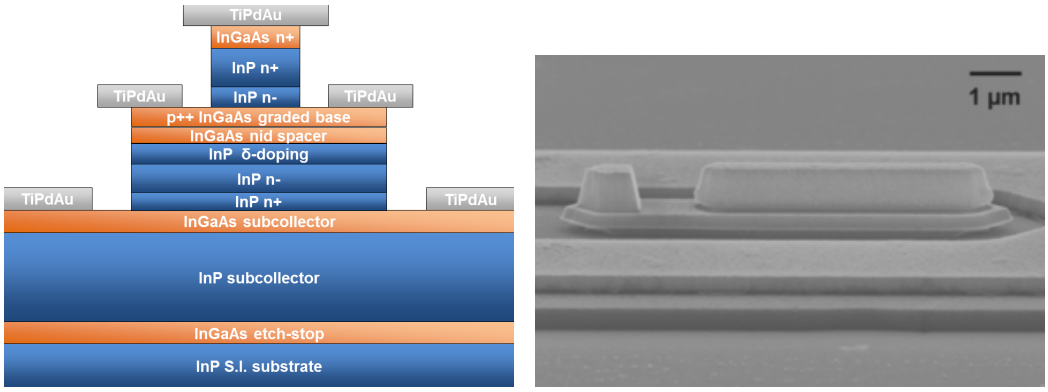
CHAPTER 2

InP DHBT Technology

Indium phosphide (InP) is an important III-V compound semiconductor with favorable physical and electronic properties for use in microwave and mm-wave devices. Some of the most important characteristics of InP are high peak electron velocity, high electric breakdown field, and relatively high thermal conductivity [39]. It is usually used as substrate for epitaxial growth of lattice-matched layers to form heterostructures for today's high performance devices. Moreover, its high resistivity makes it well suited as semi-insulating substrate for high quality passive components in MMIC designs.

The birth of heterojunction bipolar transistors (HBTs) dates back to the 1950s from an invention by Kroemer [40]. The main difference with respect to the homojunction counterpart is that the emitter is made of a different material with a wider band-gap than the base region. The desired effect is the creation of a potential barrier in the valence band which prevents minority carriers from the base diffusing into the emitter region, thus increasing the current gain. As a consequence, the base can be highly doped so as to reduce the base resistance and hence increase the maximum oscillation frequency $f_{\max}$. If another heterojunction is grown at the base-collector interface, a double HBT (DHBT) is formed. In this case, the same wide band-gap semiconductor material of the emitter is usually used for the collector so a high breakdown voltage results, which is particularly attractive for power applications [41].

To attain mm-wave and terahertz frequencies, the size downscaling of devices is a fundamental step for reducing carriers transit time and charge storage effects [42]. InP HBTs with 130 nm emitter width are currently achieving frequencies of operation into the terahertz band and a breakdown voltage $BV_{\text{ceo}} \approx 3.5\,\text{V}$ [30]. Yet another interesting InP DHBT process is that reported in [43], where a breakdown voltage of $BV_{\text{ceo}} \approx 12\,\text{V}$ and $f_{\max} = 470\,\text{GHz}$ are reported for transistors having 250 nm of emitter width. Interesting performances are also obtained by an antimonide-based InP DHBT technology [44]. With an emitter area of $0.3 \times 4.4\,\mu\text{m}^2$, these devices feature maximum oscillation frequencies in excess of 700 GHz and a breakdown voltage of 5 V.



(a) (b)

Figure 2.1: Representation of the InP DHBT develeoped at III-V Lab: (a) cross section and (b) SEM image of a single-finger device.

2.1 InP DHBT Technology at III-V Lab

The InP DHBT technology used in this work is developed at III-V Lab, France. It was first intended for high-speed mixed-signal systems and optical communications [45]. Through the years, several optimization steps have been undertaken in an attempt to ameliorate its frequency performances. A great amount of efforts have been addressed also to adapt this technology for mm-wave power amplifiers [47]. As a result, two different processes are currently available – internally denoted as *SHARC* and *SAND* processes – tailored for high-speed mixed-signal and analog power applications, respectively. A basic description of the DHBT devices from the two processes is reported in the following, including performance differences and modeling approach.

2.1.1 DHBT Structure

In Figure 2.1(a), a simplified cross section of the InP DHBT is shown and a SEM image of a single-finger device is reported in Figure 2.1(b). The epitaxial material is grown by Gas Source Molecular Beam Epitaxy (GSMBE) on a three-inch 600-μm thick semi-insulating InP substrate. The layer structure consists of a 40 nm InP emitter, a 30 nm highly carbon-doped and compositionally graded InGaAs base and a composite collector. The collector includes a non-intentionally doped (nid) InGaAs spacer, a highly doped InP region and a low doped InP layer. The low-doped InP layer is used to fully deplete the collector at low bias. The emitter width is 0.7 μm and different emitter lengths are available from 5 μm to 10 μm. In this project, dealing with power amplifiers, only 10 μm emitter lengths have been considered for the higher power capabilities.

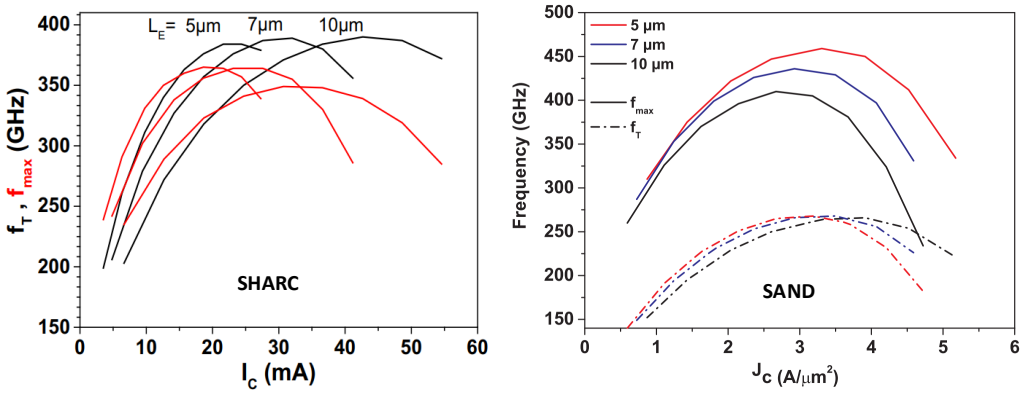
The two parameters which are always considered while evaluating transistors performances are the cutoff frequency f_T, defined as the frequency at which the ac current gain H_{21} falls to unity, and the maximum oscillation frequency $f_{\max}$, which is the frequency where the unilateral power gain U is unity. To better describe the optimization process of active devices, it is useful to recall their expressions for an HBT:

$$\frac{1}{2\pi f_T} = \tau_b + \tau_c + r_{\mathrm{E}}\left(C_{\mathrm{je}} + C_{\mathrm{bc}}\right) + \left(R_{\mathrm{E}} + R_{\mathrm{C}}\right)C_{\mathrm{bc}}, \tag{2.1}$$

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi\left(R_{\mathrm{bx}}\left(C_{\mathrm{bcx}} + C_{\mathrm{bci}}\right) + R_{\mathrm{bi}}C_{\mathrm{bci}}\right)}} \tag{2.2}$$

where τ_b and τ_c are the base and collector transit time respectively, r_{E} is the dynamic base-emitter resistance divided by the current gain β, $C_{\mathrm{bc}} = C_{\mathrm{bcx}} + C_{\mathrm{bci}}$ is the total base-collector capacitance comprising the extrinsic and intrinsic components, C_{je} is the base-emitter junction capacitance, R_{E} and R_{C} are the extrinsic emitter and collector resistances, respectively, and R_{bx} and R_{bi} are the extrinsic and intrinsic components of the base resistance R_{b}, respectively. Improving the frequency performances requires the simultaneous scaling of vertical and lateral dimensions: thinning the base and collector layers reduces the transit times τ_b and τ_c and hence increases f_T. However, if this is not accompanied by a horizontal scaling, the access resistance R_{b} and the base collector capacitance C_{bc} would increase, entailing a decrease of $f_{\max}$ [42]. On the other hand, with a given emitter width, an increase of $f_{\max}$ can be accomplished by a thicker collector giving a lower C_{bc}, provided that a slight degradation of f_T can be accepted. This has been, indeed, the approach followed in this project to tailor the available devices for power amplifier design [47]. The main parameter to be addressed in the optimization process was the thickness of the low doped n^- layer in the collector. The collector structure has been thickened to lower the parasitic capacitance and hence increase the value of the maximum oscillation frequency $f_{\max}$ and of the breakdown voltage BV_{ceo} for higher output power, while the horizontal dimensions are kept constant, with the emitter width being 0.7μm. Thickening the collector layer, however, caused a longer collector transit time τ_c which translated in a reduction of the cutoff frequency f_T. The two processes currently in production at III-V Lab, SHARC and SAND, have collector thicknesses of 130 nm and 190 nm, respectively.

The epitaxy optimization process included also a reduction of the thickness of the etch-stop InGaAs layer: as its thermal conductivity is quite poor, this layer exacerbates the self-heating



(a) (b)

Figure 2.2: Extracted f_T and $f_{\max}$ of the SHARC (a) and SAND (b) InP DHBTs with emitter width of 0.7 μm fabricated in 2015 at III-V Lab [47, 48].

mechanism, so its thinning helped in extending the safe-operating-area (SOA).

In Figure 2.2, the extracted values of f_T and $f_{\max}$ for SHARC and SAND processes are reported as functions of the bias collector current for different emitter lengths [47, 48] and constant emitter width of 0.7 μm. The SHARC process exhibits higher values of f_T than $f_{\max}$, the former approaching 400 GHz and the latter being around 350 GHz. As a result of the optimization process, the $f_{\max}$ of the SAND process is significantly improved, but at the expense of a reduction of the f_T values. The breakdown voltages BV_{ceo} has improved from 5 V to 7 V, resulting in an extended SOA.

An emerged drawback of collector thickening is an increased conduction band offset at the base-collector junction which exacerbates the current blocking mechanism [47]. Another effect is a flattening of the conduction band at the collector region. The combination of these two effects translates in a higher collector resistance and a higher knee voltage of the output characteristics for the SAND process.

2.1.2 Single-Finger Device Modeling

In Figure 2.3, the equivalent circuit model of a single-finger InP DHBT used in the design process of power amplifiers is reported. It represents the UCSD HBT model improved with a bias-dependent intrinsic collector resistance R_{ci} as demonstrated in [49]. It is implemented in Keysight ADS by means of an eleven-port symbolically defined device (SDD) component which takes into account all the physical peculiarities of HBTs such as the Kirk effect, carrier velocity modulation and self-heating. The collector current for a common-emitter configuration in forward active region operation can be expressed as:

$$I_{\text{C}} = I_{\text{S}}\left(T\right) e^{\frac{qV_{\text{be}}}{\eta kT}}, \tag{2.3}$$

where $I_{\text{S}}\left(T\right)$ is the saturation current, V_{be} is the base-emitter voltage, η is the base-emitter junction ideality factor, k is the Boltzmann constant, q is the magnitude of the electron charge and T is

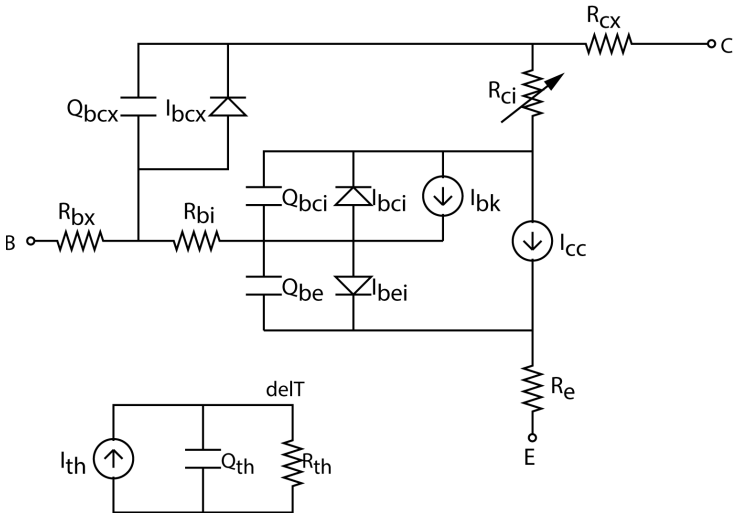


Figure 2.3: Improved large-signal UCSD HBT model of a single-finger InP DHBT.

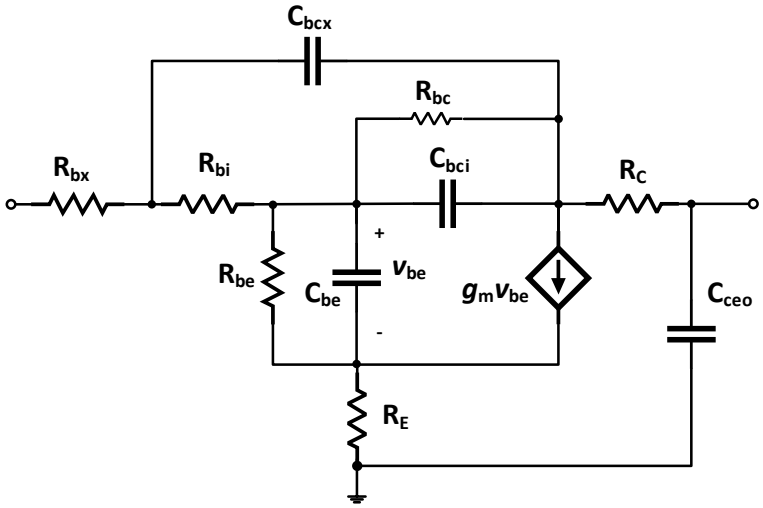


Figure 2.4: Small-signal model of a single-finger InP DHBT.

the absolute temperature. In (2.3), only the contribution of the base-emitter voltage V_{be} has been considered, while that of the base-collector voltage V_{bc} has been neglected. This is a reasonable assumption in forward active operation. The ideality factor η is particularly important for HBT modeling as it takes into account the band conduction discontinuity at the base-emitter junction. In fact, besides the drift and diffusion components which are normally present in any bipolar transistor, the spike in the conduction band may introduce other contributions such as thermionic emission and tunneling which make the ideality factor η be different from unity [49]. The above expression emphasizes the fact that the saturation current $I_{\mathrm{S}}\left(T\right)$ is temperature dependent. In turn, the transistor temperature depends on the current flowing through it. To take into account this temperature feedback mechanism, the large-signal model includes a lumped-element thermal network as well, which provides a first order estimate of the temperature rise of the transistor as it functions under high current conditions [50].

In order to evaluate the ac performances of transistors, it is useful to develop a small-signal model in correspondence of the actual bias condition under which the device is normally operated. It is often represented as a hybrid π model so that it can be easily described by small-signal Y-parameters extracted from S-parameters measurements. Figure 2.4 shows the small-signal equivalent circuit extracted following the procedure described in [51].

2.1.3 Multiple-Finger Device Modeling

Figure 2.5 shows a simplified schematic representation of the multi-finger model structure which is often used in power amplifier design. Indeed, it is made of four single-finger models embedded into a multi-port parasitic network. The most important parasitic elements are the highly inductive transmission line represented by the emitter strip and the collector to emitter overlap capacitance ΔC_0.

The simulated output DC characteristics of the four-finger device, which are extensively used in this project, are reported in Figure 2.6 for the SHARC and SAND technologies. The base current is varied in steps of 0.4 mA up to 6 mA for the SHARC device and up to 4 mA for the SAND device. The approximated maximum dissipated power establishing the SOA is also reported in the plots by the red curve, which is more realistic with respect to the simulated breakdown. In fact, the large signal model loose some accuracy in predicting the breakdown and seems quite optimistic compared with the measured results which are being shown in the following. Besides a slightly higher breakdown voltage for the SAND device, other differences that can be identified include a higher current gain and a higher knee voltage. The latter is due to the higher intrinsic collector resistance and represents a drawback for high output power as it limits the lower excursion of the output voltage swing. For Class A operation the two devices are biased at (I_C, V_{CC})=(80 mA, 2 V) and (I_C, V_{CC})=(60 mA, 2.4 V), respectively. With these bias settings, the maximum gain achievable from the two processes are reported in Figure 2.7, where the better performances of the SAND process are evident. For instance, at 80 GHz, a SAND four-finger device exhibits 9.1 dB of maximum available gain, against 6.3 dB of the SHARC counterpart. The four-finger device in the SAND process has been selected in this project for the design of power amplifiers.

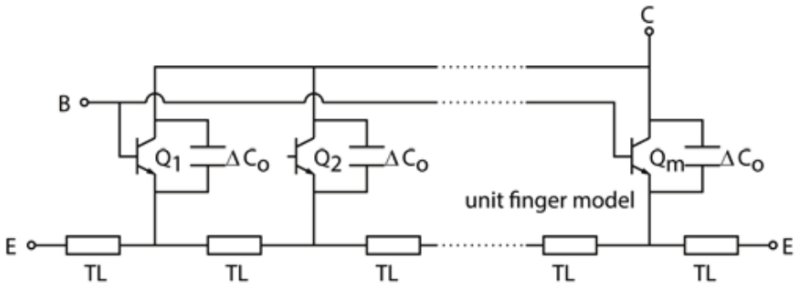


Figure 2.5: Simplified schematic representation of multi-finger model structure.

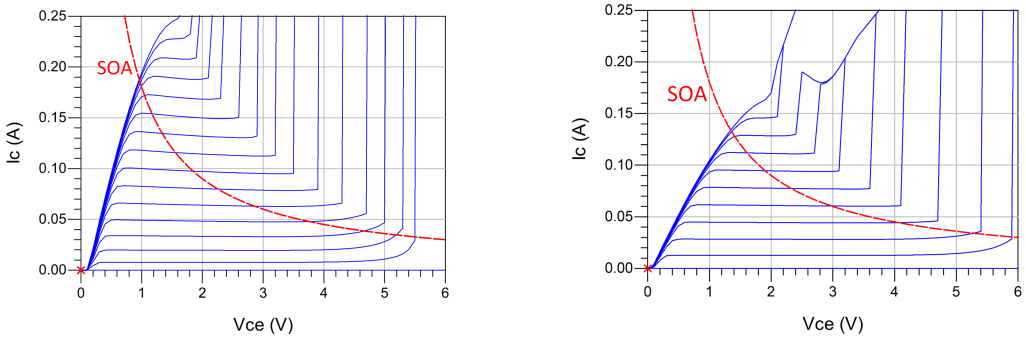


Figure 2.6: DC output characteristics of the four-finger device ($4 \times 0.7 \times 10$ μm^2) in SHARC (a) and SAND (b) technologies. The base current is varied in steps of 0.4 mA. The limit of the safe operating area is indicated by the red line.

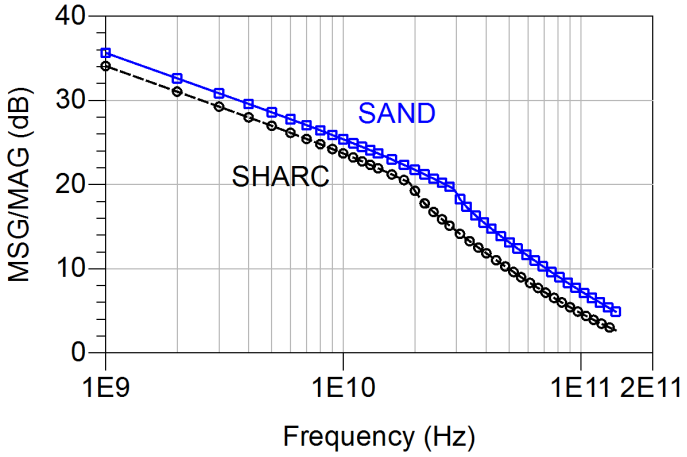


Figure 2.7: Maximum stable gain and maximum available gain of the four-finger transistor in SHARC and SAND technology biased at (I_C, V_{CC})= (80 mA, 2 V) and (I_C, V_{CC})= (60 mA, 2.4 V), respectively.

2.1.4 Emitter-Ballasted Multiple-Finger Device Modeling

Multi-finger topologies are usually employed to increase the output power of transistor configurations. However, because of their geometry and process variations, they can experience thermal instabilities under high power regimes, leading to circuit failures [52]. The mechanisms behind the onset of thermal instabilities are by now well-known and a common technique to prevent them is the use of ballasting resistors. Such a technique is employed in this technology in the way described in [47] and [53]. Ballasting resistors are connected between the emitter contacts and ground as shown in Figure 2.8 and, by acting as a negative feedback, they counteract the rising of the current flowing in the fingers in consequence of self and mutual thermal heating. A resulting effect is also that the total current is equalized among the fingers. All this leads to an extended SOA, so the bias voltage can be increased and a larger voltage swing is allowed. In the case of ballasted transistors,

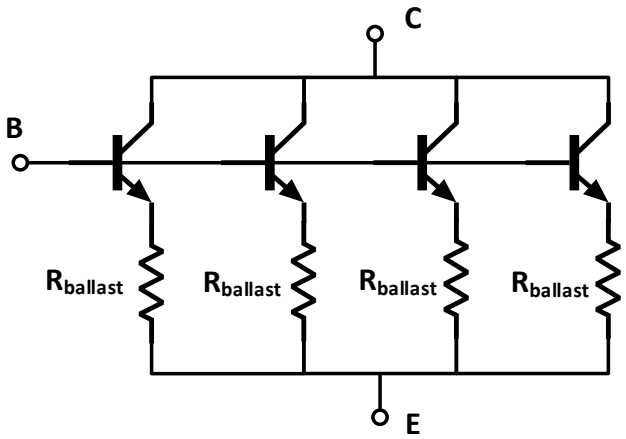
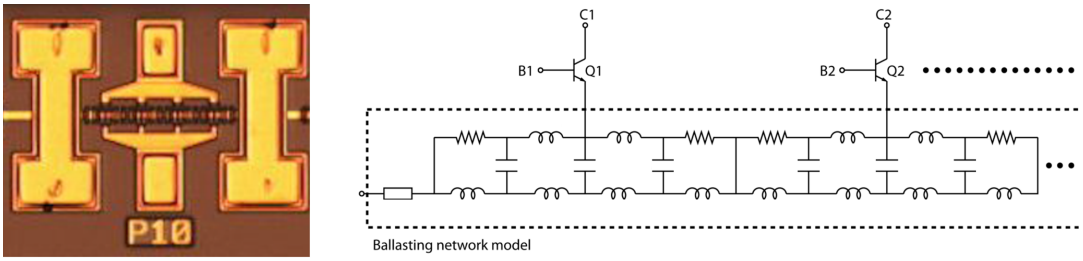


Figure 2.8: Circuit model of the ballasted multifinger transistors.



(a) (b)

Figure 2.9: Microphotograph of a four-finger ballasted devices with contact pads structure (a) and extracted physical model with lumped elements [53].

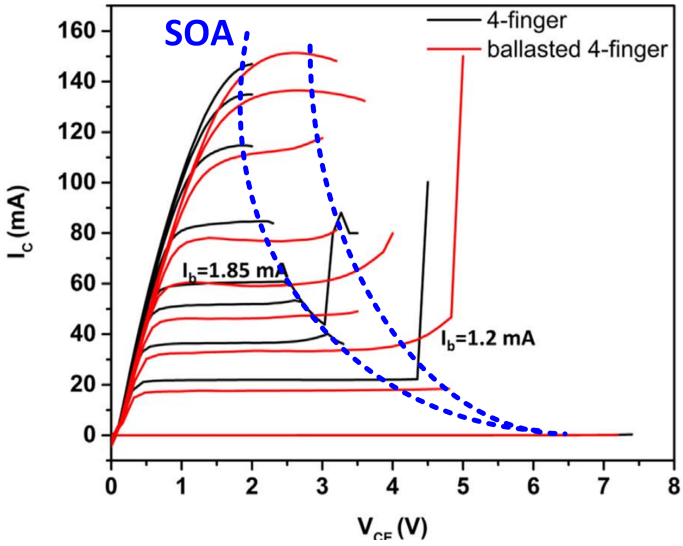


Figure 2.10: Comparison of the measured dc characteristics of a standard four-finger device and a ballasted one.

the current-voltage characteristic of (2.3) must be modified to take into account the feedback effect as:

$$I_{\mathrm{C}} = I_{\mathrm{S}} e^{\frac{1}{\eta V_{\mathrm{th}}}\left(V_{\mathrm{be}} + \Phi R_{\mathrm{th}} I_{\mathrm{C}} V_{\mathrm{ce}} - I_{\mathrm{C}} R_{\mathrm{E,total}}\right)}, \tag{2.4}$$

where $V_{\mathrm{th}} = kT/q$ is the thermal voltage, R_{th} is the self-heating thermal resistance of a single-finger device, and

$$\Phi = \frac{-\partial V_{\mathrm{be}}}{\partial T} \tag{2.5}$$

is the thermal electric feedback coefficient defined in [52]. From (2.4), it results that, in order to avoid thermal effects, the following condition must be satisfied:

$$R_{\mathrm{E,total}} = \Phi R_{\mathrm{th}} V_{\mathrm{ce}}, \tag{2.6}$$

where $R_{\mathrm{E,total}} = R_{\mathrm{E}} + R_{\mathrm{ballast}}$ is the total emitter resistance of the ballasted transistor. The choice of the value of R_{ballast} is critical: a high value leads to a pronounced feedback effect and is

desirable for thermal stability, but it significantly reduce the power gain [55]. It has been found and discussed in [47] that the optimum value for the present InP DHBT technology is 5 Ω.

The simple schematic of the ballasted transistor shown in Figure 2.8 is a conceptual one. In reality, the interconnects of the various components must be taken into account for accurate modeling. A more realistic and detailed model of the ballasted transistor is shown in Figure 2.9(b), which has been extracted from S-parameter measurements being aware of the particular layout configuration and parasitics. In Figure 2.9(a), the microphotograph of a ballasted transistor is shown with its pad structure for measurements purpose. To evaluate the improvements of the power capabilities, its output characteristics are compared with those of a standard device as reported in Figure 2.10, where a SOA extension of ≈ 1 V can be seen.

2.2 Passive Structures

Figure 2.11 shows a pictorial representation of the back-end-of-line (BEOL) process of III-V Lab's InP DHBT technology. In order to characterize all passive structures and particular layout configurations, it has been modeled in Keysight ADS for 2.5D electromagnetic (EM) simulations carried out in Momentum. The modeled representation is shown in Figure 2.12. It is based on the three TiPdAu metal layers (*met1-met3*) with conductivity $\sigma = 3.33 \times 10^7$ S/m and thicknesses of 0.58 μm for *met1* and 1.2 μm for *met2* and *met3*. They are separated by thin polyimide layers with relative permittivity $\epsilon_r = 2.9$ and thicknesses of 0.8 μm (between *met1* and *met2*) and 1.2 μm (between *met2* and *met3*). Dielectric and conductive losses into the polyimide layer are taken

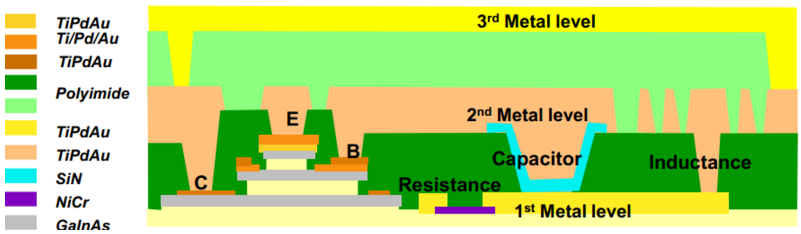


Figure 2.11: Representation of the InP back-ene-of-line.

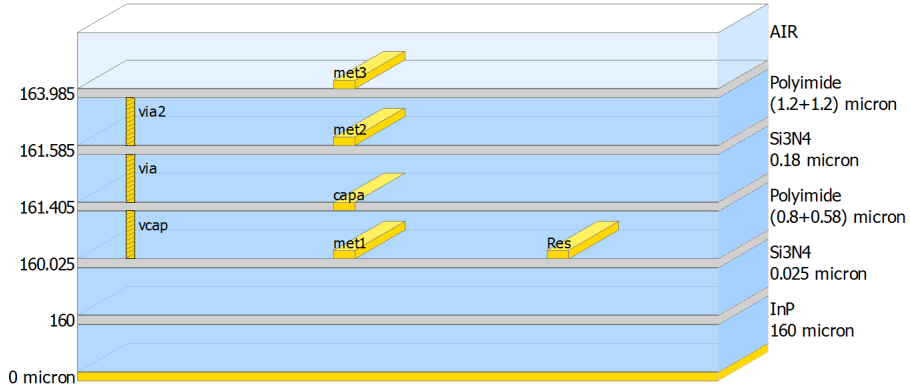


Figure 2.12: Layer-stack modeling in Keysight ADS for EM-simulation of passive structures.

into account by setting the dissipation factor $tan\delta = 0.005$ and forcing it to follow the Svensson-Djordjevic model to account for the variations in the frequency domain [56, 57]. Thin-film resistors (TFR) are realized by means of a NiCr layer having a resistivity of 40 $\Omega/\square$. A thin (0.18 μm) Si_3N_4 insulating layer is also available for metal-insulator-metal (MIM) capacitors between *met1* and *met2* having a capacitance per unit area of 0.49 fF/μm^2.

Several transmission line topologies could be used for matching networks and power combining implementations. The conventional microstrip line technology, consisting of a topside metal strip and a metal ground on the backside of the substrate, is not feasible in this technology. Even though the InP substrate is thinned down to 160 μm to avoid parasitic modes, at mm-waves this is still a considerable thickness comparable to the wavelength; any ground connection would require a strongly inductive via hole through the substrate. Moreover, a 50-Ω transmission line with this approach would require a too wide top metal strip which would limit on-chip integration. For all these reasons, the conventional microstrip is discarded. Instead, all transmission lines must be implemented on the topside of the process by means of thin-film structures. In this regard, several investigations have been conducted in order to establish the most suitable solution taking into account many aspects, such as losses, dispersion, integration and, not least, ease of implementation.

A thin-film microstrip line (TFML) with signal strip on *met3* and ground on *met1* or *met2* is quite impractical because many ground cuts and discontinuities would be necessary to accommodate transistor devices and other passive components. A viable alternative could be the inverted TFML realized with the ground plane on *met3* and the signal trace on either *met1* or *met2*. Because of the very thin polyimide layers, a characteristic impedance of 50 Ω would require signal strips very narrow which could result in significant conductive losses. EM-simulations have been carried out for both cases in order to estimate the performances of inverted TFML structures having around 50 Ω of characteristic impedance. In the former case (signal trace on *met1*), this value is obtained with a trace width of 4 μm, corresponding to the minimum feature size established by the design rules of the technology. In the second case (signal trace on *met2*), with the same trace width, a much

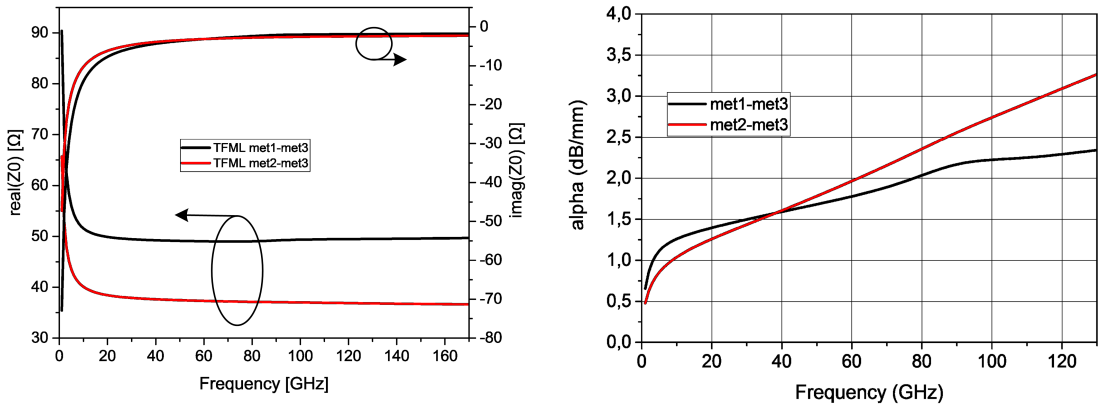


Figure 2.13: Characteristic impedance (a) and attenuation constant α extracted from EM-simulation of the inverted TFMLs with signal trace on *met1* and *met2* with ground on *met3*.

lower characteristic impedance could be achieved because of the thinner dielectric. In Figure 2.13, the characteristic impedance Z_0 and the attenuation constant α of the two inverted TFMLs are compared. After EM-simulations and extraction of the $ABCD$-matrices, they have been calculated as:

$$Z_0 = \sqrt{\frac{B}{C}} \tag{2.7}$$

and

$$\alpha = \cosh^{-1}\left(\frac{A}{l}\right), \tag{2.8}$$

where l is the lenght of the line. As can be seen, both structures exhibit significant losses, especially the one with the signal trace on *met2* and thinner dielectric. Such narrow lines result also problematic in the eventuality of handling dc currents and withstand electromigration issues. Thus, they are not really favorable for MMIC implementations on this technology and other approaches have been studied.

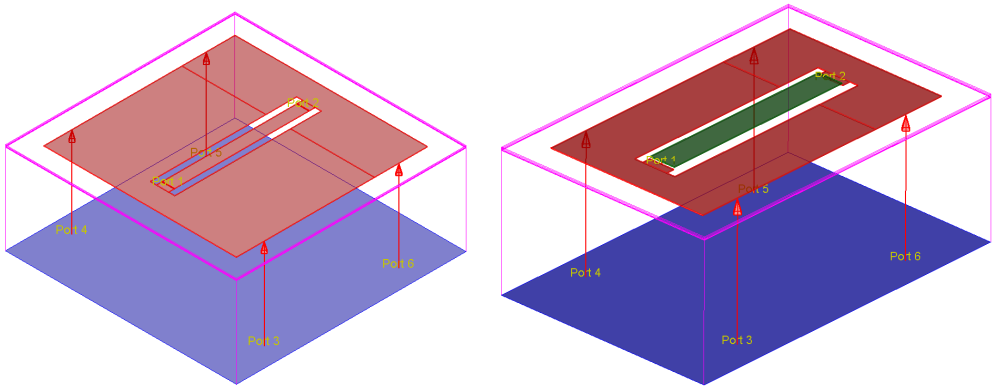
An alternative which is attracting considerable interest in MMIC design is the coplanar waveguide (CPW) structure. This configuration has at least two degrees of freedom (namely the width of the central conductor and the ground-to-ground spacing) for realizing a given value of characteristic impedance. A good tradeoff between these two parameters should guarantee low loss and reasonable size for on-chip integration. In III-V Lab's InP technology, the best compromise has been found in a central conductor width of 22 μm and a ground-to-ground spacing of 44 μm arranged on *met2*, resulting in a characteristic impedance of $Z_0 \approx 50\Omega$. The wider central conductor in comparison with the thin-film microstrip ensures lower conductive losses. Other advantages of the CPW are a lower dispersion and an increased effective permittivity, which allow for a shorter line with the same electrical length.

Based on the described features of the two technologies investigated (inverted TFML and CPW), the CPW has been selected for the realization of matching networks and power combiners.

A comparison can be made against the current state-of-the-art process. The InP BEOL of Teledyne's process, for instance, can be better exploited for the implementation of thin-film microstrips. They can leverage a 7-μm BCB layer between *met1* and *met3* and a 3-μm thick top metal layer [30]. The higher inter-metal spacing, which allows for a wider signal trace for a given impedance, and the thicker metals guarantee lower losses.

2.2.1 Design-Kit

A remarkable difficulty in dealing with thin-film CPW on a multilayer technology is the lack of an accurate modeling for most CAD tools, in contrast with microstrip lines which are available with parametrized dimensions in most design-kits. Thus, MMIC designs based on CPW technology must often rely on EM simulations, resulting in a lengthy and cumbersome process whenever a change has to be made on the circuit topology. In order to mitigate this issue, a library of basic passive components previously characterized by EM-simulations and relative Touchstone files have been developed for III-V Lab's InP technology for use in Keysight ADS environment. All circuit designs are then based as much as possible on them, except in the case when a particular cell topology is needed.



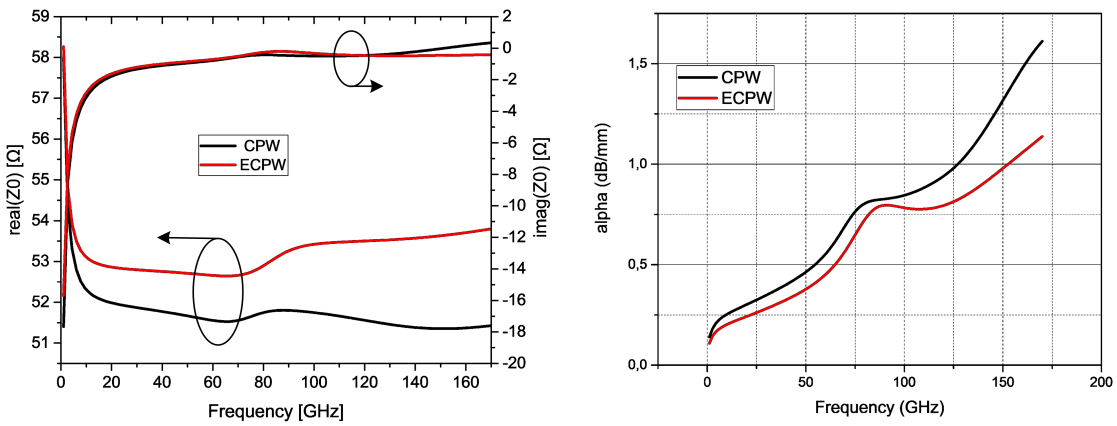
(a) (b)

Figure 2.14: Layout and EM-simulation setup of the CPW (a) and ECPW (b) in a ground ring excitation scheme.

In what follows, a description of the developed design-kit components and their characterization is briefly described. They include 50 Ω transmission lines, series and shunt MIM capacitors, open and shorted stubs, and discontinuities such as bending, tee and cross structures. Accurate analysis and parameter extraction have been carried out following the procedure described in [58] based on 2.5D EM simulations with ground ring excitation schemes performed on ADS Momentum and extended double delay (L-2L) calibration method.

50 Ω CPW Transmission Line

The ADS library contains standard CPW lines with 22 μm trace width and 44 μm ground-to-ground spacing which results in a characteristic impedance of $Z_0 \approx 50\Omega$. An elevated CPW (ECPW) with the central trace on *met3* and ground plane on *met2* has been also developed in an



(a) (b)

Figure 2.15: Attenuation constant α extracted from EM-simulation of the CPW and ECPW lines.

attempt to reduce conduction losses by means of a wider signal trace of 32 μm and ground-to-ground spacing of 54 μm, which approximately results in the same characteristic impedance. In Figure 2.14, the layout and EM-simulation setup with ground ring excitation schemes for the two type on lines are shown. In Figure 2.15, the comparison of the characteristic impedance Z_0 and attenuation constant α of the two types of CPW lines are reported as a function of frequency. As can be seen from the plot, the ECPW line exhibits lower loss than the CPW line over the whole simulation frequency range. In the E-band range, however, this advantage is less pronounced. In circuit implementations, where the lines are far shorter than 1 mm, the difference between using one or the other is minimal. 50 Ω CPW and ECPW are provided in the design-kit as circuit components for schematic level design with parametric length and fixed width.

Discontinuities

In order to accurately predict the circuit performances, matching networks must be accurately modeled. At mm-waves, even small parasitic elements not carefully taken into account can negatively impact the design. The InP DHBT library includes also the models of some frequently used components such as tee junctions, bendings, short and open terminations which have been extracted from EM-simulations. The 3D layout representation of some discontinuity components which are widely used are shown in Figure 2.16, where the de-embedding reference planes are reported as well. The simulated losses associated to the bending structure are approximately 0.2 dB at 80 GHz. For the tee-junction the attenuation from port 1 to port 2 is around 0.6 dB while the attenuation from port 1 to port 3 is around 0.8 dB at 80 GHz.

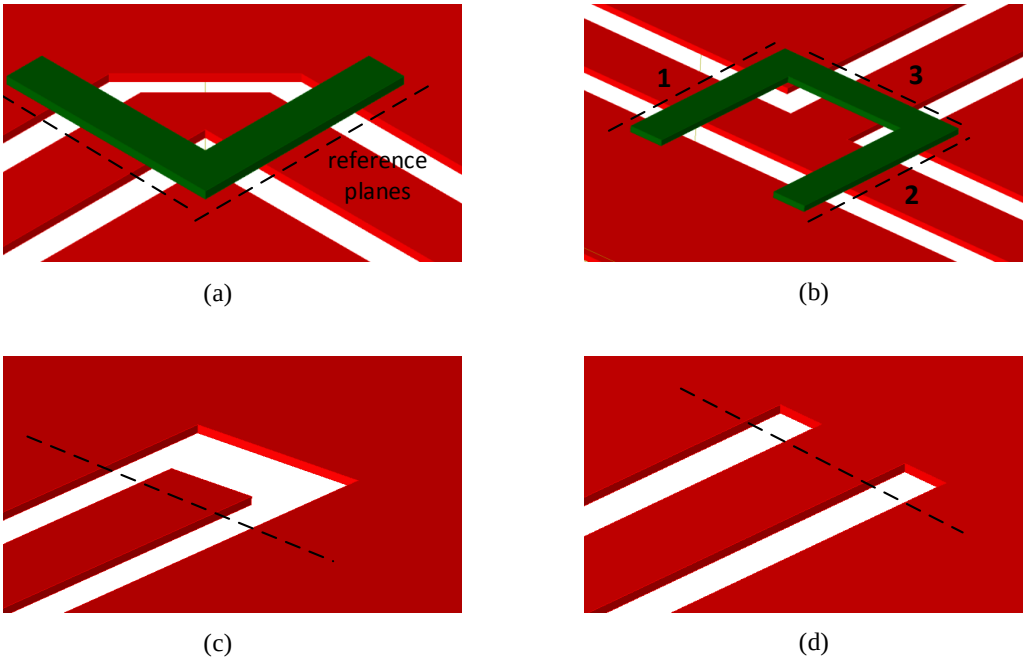


Figure 2.16: 3D layout view of some discontinuities available in the design-kit: (a) bending, (b) tee-junction, (c) open, (d) short.

MIM Capacitors

Some specified values of MIM capacitors in both series and shunt configurations are also modeled and available in the schematic design environment. Their models are also derived from S-parameters extracted from EM-simulation. In Figure 2.17, the 3D layout of series and shunt capacitors are shown. The two components are fed by the same CPW line shown above and placed in a ground opening whose dimensions are dictated by the technology design rules. In order to prevent the onset of parasitic slot-line modes in correspondence of the ground discontinuities, the ground planes are connected by means of air bridges. In extracting the model of the MIM capacitors, a deembedding procedure has been used to remove the contribution of the CPW lines feeding the components. The reference planes have been chosen as shown in Figure 2.17. The losses associated with the series capacitance are 0.4 dB and are approximately constant for frequencies higher than 40 GHz.

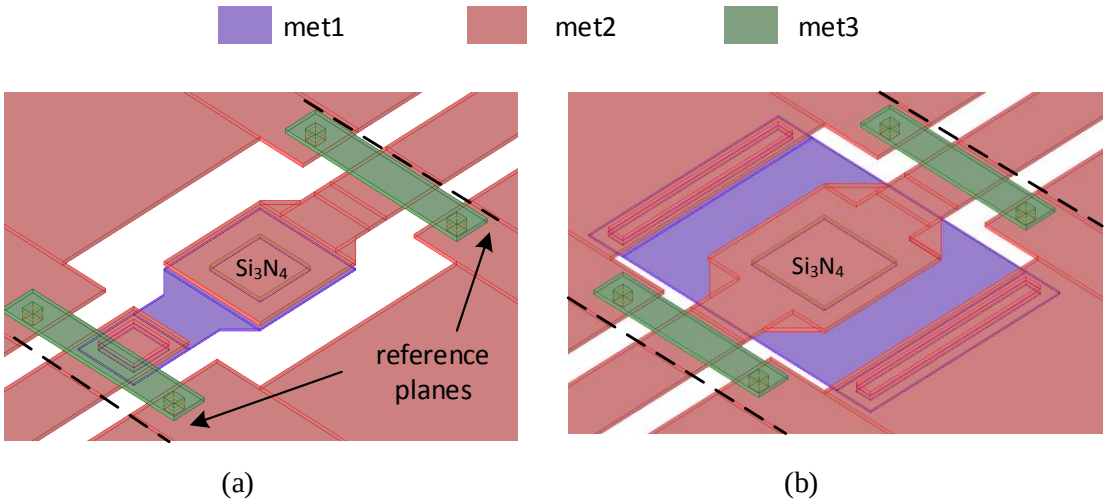


Figure 2.17: 3D layout view of a series (a) and shunt (b) capacitors available in the III-V Lab's InP DHBT design-kit.

2.3 Summary

The main characteristics and performances of the III-V Lab's InP DHBT technology used in this project have been reported in this chapter. An introduction to the most important physical properties determining the high frequency performances of transistors has been given. The SHARC and SAND processes have been introduced highlighting their technological and related performance differences for the sake of better understanding the behavior of the fabricated power amplifiers which are presented in the following. Thanks to the thicker collector layer of the SAND process, higher values of $f_{\max}$ and BV_{ceo} can be achieved, making it better suited for power applications. The UCSD transistor model used for simulation purposes is also briefly described.

To alleviate the thermal issues affecting the power performance of multifinger transistors, a ballasting resistive network connected to the emitter contacts has been introduces. Besides the fundamental theoretical explanation, measurement results have been shown with significant improvement of the SOA for ballasted transistors, though their maximum gain could be lower due to the extra resistive losses. An interesting application where such a configuration has been successfully applied is the common-base stage of a stacked-transistor architecture which is described in the following chapter.

An illustration of the back-end-of-line (BEOL) and passive components has been given as well. The choice of CPWs for implementing the matching networks and most of the interconnects has been motivated by practical issues and lower losses. The thin-film microstrip line (TFML) alternative revealed too lossy and impractical on this particular technology. For instance, at 80 GHz, the CPW exhibits around 0.8 dB/mm of attenuation, against more than 2 dB/mm for the TFML counterpart. A short description of the in-house developed design-kit is finally given with an illustration of the most used components: bendings, tee-junctions, short and open stubs, and MIM capacitors.

Thus, this chapter constitutes an important starting point for contextualizing and understanding the design approach and implementation of the realized MMIC power amplifiers. Such an acquaintance with the technology is of fundamental importance for the interpretation of the experimental results.

CHAPTER 3

Stacked-Transistor Topology

3.1 Introduction

The continuous size downscaling of devices allows to operate at mm-wave and higher frequencies [18], but this entails also a reduction of the sustainable operating voltages and output power, as predicted by the Johnson limit [14]. Power combining techniques are often needed to reach acceptable levels of transmitted power. Parallel current combining architectures represent the mainstream in this regard, but their limited bandwidth and moderate losses can impair the power amplifier performance. Moreover, their relatively large chip-area occupancy might be an issue. A viable alternative is the series voltage combining technique, known as stacked-transistor, where individual voltage swings of the single transistors are summed up in phase while the current swing remains approximately unchanged in comparison with a single-device power cell. If n is the number of transistors connected in series, this results in an overall output power n times higher. Another potential benefit is that the optimum output load, defined as the ratio between the maximum voltage and current swings, also increases by the same factor, allowing a wider bandwidth and lower losses in the matching network. The stacked-transistor topology consists of a common-emitter (or common-source) stage followed by a series of $n-1$ common-base (or common-gate) stages. It differs from the cascode because finite impedances are connected to the base of the common-base stages, making the base terminals experience a voltage swing to prevent base-collector breakdown. Collector-emitter breakdown is avoided by making the overall output voltage be equally divided among all the devices. This architecture has been successfully deployed at RF and microwave frequencies since its conception a couple of decades ago [59, 60, 61, 62, 63, 64, 65], showing promising performances in terms of output power, gain, and efficiency. More recently, many research efforts have been exerted to extend the stacked-transistor concept at higher frequencies and into the millimeter-wave range [23, 67, 68, 69, 70, 71]. An important condition to be satisfied for optimal performance of the stacked-transistor amplifier is the interstage impedance matching between all the devices so as to limit internal reflections and power degradation. This aspect has been particularly emphasized in previous works and detailed analysis for calculating the common-base input impedance have been carried out. For operating frequencies much less than the cut-off frequency f_T, the transistors' reactive components have been neglected without significant loss

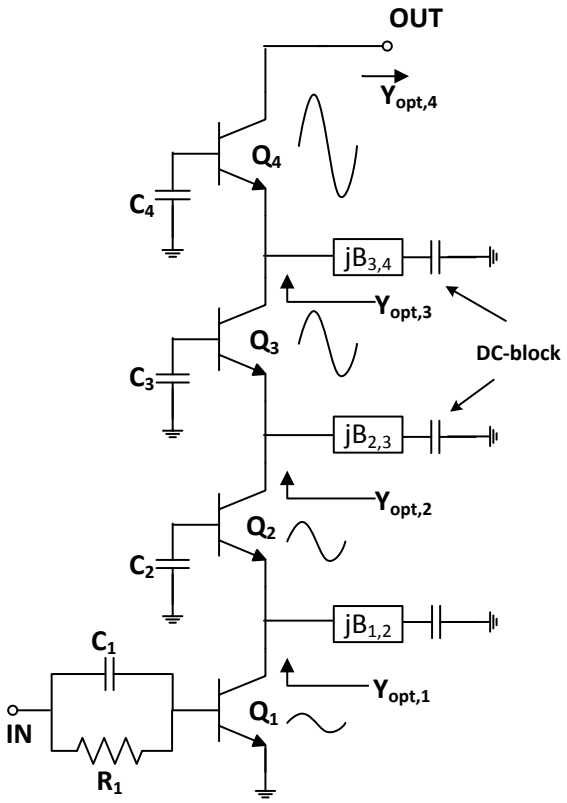


Figure 3.1: Conceptual circuit schematic of a four-stacked transistor power cell.

of accuracy [61]. At high millimeter-wave frequencies, however, this simplification does not hold and layout-related parasitics must be characterized through EM simulations and taken into account as well [23, 70]. Several strategies have been proposed to accomplish the interstage matching condition, comprising series or parallel shunt inductive tuning and capacitive shunt-feedback tuning [67]. The stacked-transistor technique has been used mostly to overcome the limited breakdown voltage of silicon-based devices and GaAs HEMTs. Only a few works are focused on applying this approach to InP DHBTs [72, 73, 74]. These are proved to be well-suited for power amplifiers at high millimeter-wave frequencies thanks to high values of f_T and $f_{\max}$, as well as moderately high breakdown voltage [30]. In this project, the stacking concept has been extended to this technology to exploit even further its capabilities. Three-stacked and four-stacked power cells have been realized and measured for operation in the upper range of the E-band.

3.2 Circuit Analysis and Design

Figure 3.1 shows a conceptual schematic of a four-stacked transistor power cell ($n = 4$). It is composed of a common-emitter stage Q_1 followed by a series of three common-base stages Q_2-Q_4. For optimum output power and avoiding collector-emitter breakdown, all the devices must operate in phase under maximum voltage and current swing conditions. Base-collector breakdown is avoided by making all the base terminals oscillate with proper amplitude and phase, which

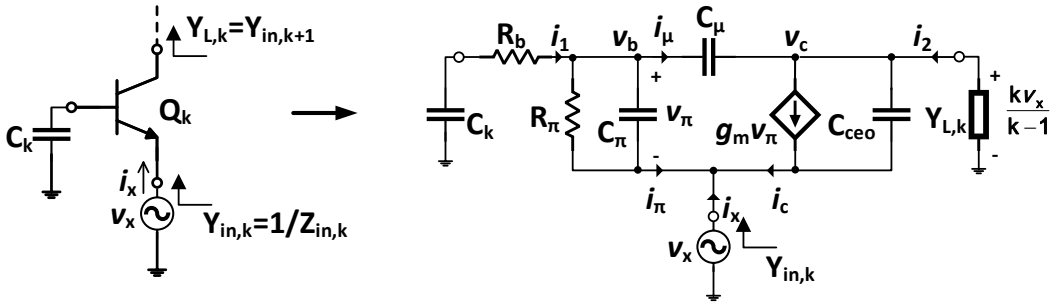


Figure 3.2: InP DHBT small-signal equivalent circuit of the k-th common-base stage for calculation of the input admittance $Y_{\mathrm{in,k}}$. Extracted parameters for a single-finger device with emitter area of $10 \times 0.7\,\mu\mathrm{m}^2$ are: $R_{\mathrm{b}} = 21.1\ \Omega$, $R_{\pi} = 110\ \Omega$, $C_{\pi} = 129.1$ fF, $C_{\mu} = 10.7$ fF, $C_{\mathrm{ceo}} = 4.9$ fF, and $g_{\mathrm{m}} = 403$ mS.

is accomplished with the base capacitances C_2-C_4 providing finite impedances, in contrast with classical cascode implementation, where the base terminals are dynamically grounded. The base capacitances C_{k}, together with the susceptances $B_{\mathrm{k-1,k}}$ ($k = 2, 3, 4$), play also an important role for interstage impedance matching between the transistors. The parallel R_1-C_1 is essential to stabilize the circuit at low frequencies. In order to easily separate real and imaginary parts in the interstage matching design, admittances are considered instead of impedances so that the shunt parasitic capacitances are more easily tuned out. The bias network is omitted in the figure, but it should be noted the all transistors must operate with the same quiescent point, and since they are dc-coupled, a relatively high bias voltage could be required. In this section, we outline the theoretical relationships and the design procedure for properly dimensioning the circuit parameters for optimum operation. First, a calculation based on an approximated small-signal equivalent circuit is given. A more practical approach based on the large signal-model is described afterward and the real design with layout considerations will be finally presented.

3.2.1 Small-signal analysis

The small-signal analysis of the stacked architecture is essential to understand the design principles. Like previous works on this subject, it can be conducted by considering the k-th common-base stage for assessing its emitter input admittance $Y_{\mathrm{in,k}}$, which must be equal to the optimum load of the preceding partial stack $Y_{\mathrm{opt,k-1}}$ [65, 70, 73]. In doing so, we refer to Figure 3.2, where a test voltage source v_{x} is applied to the emitter terminal and the resulting current i_{x} is evaluated. The interstage susceptance $B_{\mathrm{k-1,k}}$ has been omitted in the figure as it can be considered separately as a mean to resonate the imaginary part of $Y_{\mathrm{opt,k-1}}$, so at the beginning only the real part $\Re\,[Y_{\mathrm{in,k}}]$ is of concern. The illustrated small-signal equivalent circuit corresponds to a single-finger InP DHBT biased at $V_{\mathrm{ce}} = 2$ V and $I_{\mathrm{c}} = 20$ mA, whose parameters have been extracted from measured *S*-parameters following the procedure described in [51]. Some simplifying assumptions are made: we neglected in this representation the distributed nature of the base resistance and of the base-collector capacitance, so we assumed $R_{\mathrm{b}} = R_{\mathrm{bx}} + R_{\mathrm{bi}}$ and $C_{\mu} = C_{\mathrm{bcx}} + C_{\mathrm{bci}}$, where R_{bx}

and R_{bi} are the extrinsic and intrinsic base resistances, respectively, and C_{bcx} and C_{bci} are the extrinsic and intrinsic base-collector parasitic capacitances, respectively. We assumed also that the emitter resistance R_{E} and the collector resistance R_{C} are small enough to be neglected. It should be noted that in this analysis, differently from some previous works, the feedback effects introduced by C_{μ} and C_{ceo} are carefully taken into account. At millimeter-wave frequencies, in fact, these represent an important contribution to the calculation of $Y_{\mathrm{in,k}}$, which strongly depends on the load admittance $Y_{\mathrm{L,k}}$. The relationship between the collector voltage v_{c} and the emitter voltage v_{x}, corresponding to the required voltage gain for in-phase voltage addition of the k-th common-base stage, is explicitly shown in the figure. In mathematical form, the following three conditions must be met simultaneously:

$$\begin{cases} \Re\left[Y_{\mathrm{in,k}}\right] = \Re\left[Y_{\mathrm{opt,k-1}}\right] & \text{(3.1a)} \\ \Re\left[\dfrac{v_{\mathrm{c}}}{v_{\mathrm{x}}}\right] = \dfrac{k}{k-1} \qquad (k = 2, .., n) & \text{(3.1b)} \\ \Im\left[\dfrac{v_{\mathrm{c}}}{v_{\mathrm{x}}}\right] = 0 & \text{(3.1c)} \end{cases}$$

Applying KCL to the equivalent circuit of Figure 3.2 gives:

$$\begin{cases} i_{\mathrm{x}} + i_{\pi} + i_{\mathrm{c}} = 0 & \text{(3.2a)} \\ i_{\mathrm{c}} = i_{\mu} + i_{2} & \text{(3.2b)} \\ i_{1} = i_{\mu} + i_{\pi} & \text{(3.2c)} \\ i_{\mathrm{x}} + i_{1} + i_{2} = 0 & \text{(3.2d)} \end{cases}$$

The single currents can be expressed as functions of the node voltages:

$$i_{\mathrm{c}} = g_{\mathrm{m}}\left(v_{\mathrm{b}} - v_{\mathrm{x}}\right) + sC_{\mathrm{ceo}}\left(v_{\mathrm{c}} - v_{\mathrm{x}}\right) \tag{3.3}$$

$$i_{\pi} = \left(v_{\mathrm{b}} - v_{\mathrm{x}}\right)/Z_{\pi} \tag{3.4}$$

$$i_{\mu} = sC_{\mu}\left(v_{\mathrm{b}} - v_{\mathrm{c}}\right) \tag{3.5}$$

$$i_{1} = -v_{\mathrm{b}}/Z_{\mathrm{b}} \tag{3.6}$$

$$i_{2} = -v_{\mathrm{c}}Y_{\mathrm{L,k}} \tag{3.7}$$

where $Z_{\mathrm{b}} = R_{\mathrm{b}} + 1/(sC_{\mathrm{k}})$, $Z_{\pi} = R_{\pi}/(1 + sC_{\pi}R_{\pi})$ and $s = j\omega$. Here we try to express the collector voltage v_{c} as a function of the circuit parameters and the voltage source v_{x}. Using (3.3), (3.5) and (3.7) into (3.2b), the collector voltage can be written as

$$v_{\mathrm{c}} = \frac{sC_{\mu}\left(v_{\mathrm{b}} - v_{\mathrm{c}}\right) - g_{\mathrm{m}}\left(v_{\mathrm{b}} - v_{\mathrm{x}}\right) - sC_{\mathrm{ceo}}\left(v_{\mathrm{c}} - v_{\mathrm{x}}\right)}{Y_{\mathrm{L,k}}}. \tag{3.8}$$

In order to eliminate v_{b} from this expression, we can use the following equivalent relationships:

$$\left(v_{\mathrm{b}} - v_{\mathrm{x}}\right) = -\left[\frac{v_{\mathrm{b}}}{Z_{\mathrm{b}}} + sC_{\mu}\left(v_{\mathrm{b}} - v_{\mathrm{c}}\right)\right] Z_{\pi} \tag{3.9}$$

$$\left(v_{\mathrm{b}} - v_{\mathrm{c}}\right) = \frac{v_{\mathrm{x}}Z_{\mathrm{b}} - v_{\mathrm{c}}\left(Z_{\mathrm{b}} + Z_{\pi}\right)}{Z_{\mathrm{b}} + Z_{\pi} + sC_{\mu}Z_{\mathrm{b}}Z_{\pi}} \tag{3.10}$$

$$v_{\mathrm{b}} = \frac{v_{\mathrm{x}}Z_{\mathrm{b}} + v_{\mathrm{c}}sC_{\mu}Z_{\mathrm{b}}Z_{\pi}}{Z_{\mathrm{b}} + Z_{\pi} + sC_{\mu}Z_{\mathrm{b}}Z_{\pi}}, \tag{3.11}$$

so that, after some algebraic manipulation, (3.8) can be rewritten as

$$v_{\mathrm{c}} = \frac{\left[\left(sC_{\mu} + sC_{\mathrm{ceo}}\right) Z_{\mathrm{b}} + \left(g_m + sC_{\mathrm{ceo}}\right)\left(1 + sC_{\mu} Z_{\mathrm{b}}\right) Z_{\pi}\right]}{\left(Y_{\mathrm{L,k}} + sC_{\mathrm{ceo}}\right)\left(Z_{\mathrm{b}} + Z_{\pi} + sC_{\mu} Z_{\mathrm{b}} Z_{\pi}\right) + sC_{\mu}\left(Z_{\mathrm{b}} + Z_{\pi} + g_{\mathrm{m}} Z_{\mathrm{b}} Z_{\pi}\right)} v_{\mathrm{x}}. \tag{3.12}$$

In order to find the expression for the input emitter admittance $Y_{\mathrm{in,k}}$, we can consider the equation (3.2d). Using (3.6), (3.7) and (3.11), it can be rewritten as

$$i_{\mathrm{x}} = \frac{sC_{\mu} Z_{\pi} v_{\mathrm{c}} + v_{\mathrm{x}}}{Z_{\mathrm{b}} + Z_{\pi} + sC_{\mu} Z_{\mathrm{b}} Z_{\pi}} + v_{\mathrm{c}} Y_{\mathrm{L,k}}. \tag{3.13}$$

In order to find an expression dependent only on v_{x}, we could use (3.12). However, for the present case, we must have $v_c = k v_{\mathrm{x}} / (k-1)$, so we can write (3.13) as:

$$i_{\mathrm{x}} = \left[\frac{sC_{\mu} Z_{\pi} \frac{k}{k-1} + 1}{Z_{\mathrm{b}} + Z_{\pi} + sC_{\mu} Z_{\mathrm{b}} Z_{\pi}} + \frac{k}{k-1} Y_{\mathrm{L,k}}\right] v_{\mathrm{x}} \tag{3.14}$$

which finally yields the formula to calculate the input admittance.

At a given frequency and for a given transistor model, it can be seen that (3.1) is a system of three equations in the three unknowns C_{k}, $G_{\mathrm{L,k}} = \Re\left[Y_{\mathrm{L,k}}\right]$ and $B_{\mathrm{L,k}} = \Im\left[Y_{\mathrm{L,k}}\right]$, which can be solved with the aid of a numerical computing environment and verified with a circuit simulator. The calculated values of the unknown parameters are reported in Figure 3.3(a) and Figure 3.3(b) as functions of the stack number k at different frequencies for a single-finger InP DHBT with emitter area of $10 \times 0.7\ \mu\mathrm{m}^2$. It can be observed that both the base capacitance C_{k} and the load admittance $Y_{\mathrm{L,k}}$ decrease as the stack number k and frequency increase.

The value of the interstage shunt susceptance $B_{\mathrm{k-1,k}}$ is then calculated for conjugate matching:

$$B_{\mathrm{k-1,k}} = -\Im\left[Y_{\mathrm{opt,k-1}}\right], \tag{3.15}$$

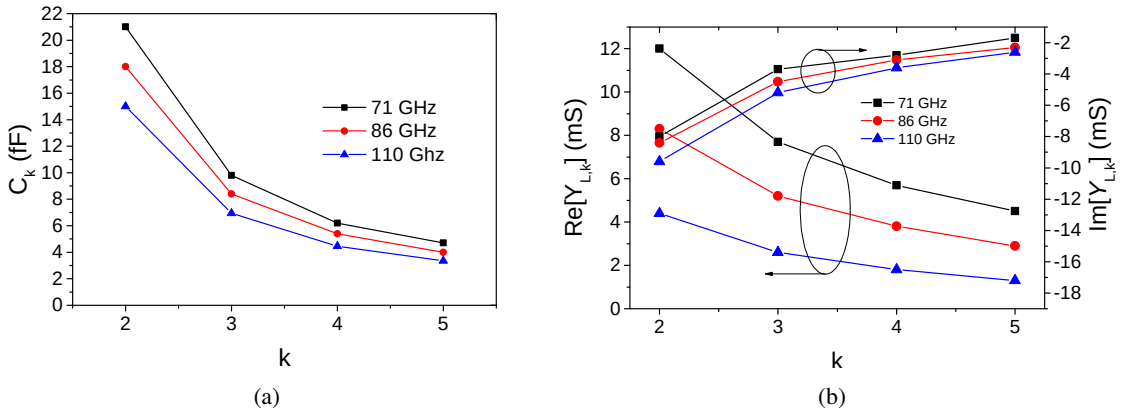


Figure 3.3: Theoretical values of the base capacitance C_{k} (a) and output admittance $Y_{\mathrm{L,k}}$ (b) of the k-th common-base stage as functions of the stack number k at different frequencies of operation for a single-finger InP DHBT with $R_{\mathrm{b}} = 21.1\ \Omega$, $R_{\pi} = 110\ \Omega$, $C_{\pi} = 129.1$ fF, $C_{\mu} = 10.7$ fF, $C_{\mathrm{ceo}} = 4.9$ fF, and $g_{\mathrm{m}} = 403$ mS.

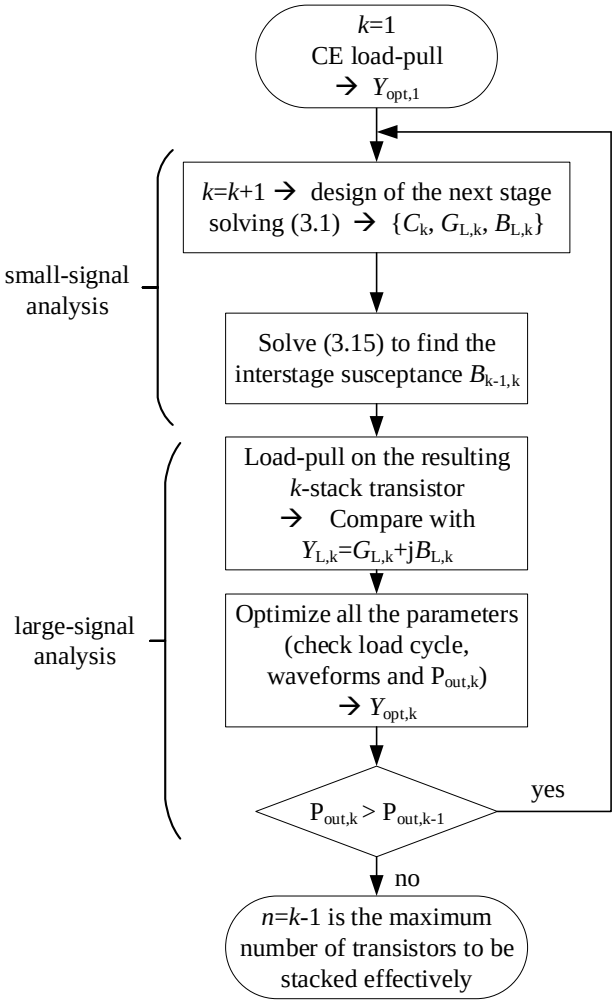


Figure 3.4: Structured flow-chart for the design of an n-stacked transistor power cell.

which is often implemented by means of an inductor $L_{\mathrm{k}-1,\mathrm{k}}$ to tune out the output parasitic capacitance of the $(k-1)$-th transistor. The latter condition ensures that the same current flows through all the devices.

3.2.2 Large-signal analysis

The above small-signal analysis is essential to get a useful understanding of the stacked-transistor concept and it is used to make a first estimation of the circuit parameters. However, it represents an idealization as real power amplifiers work in large signal regime, near or well into saturation. Moreover, additional parasitics might be present, especially in multifinger devices which are usually preferred to get higher power performances. A follow-up simulation using harmonic balance and large-signal transistor models is necessary in order to capture nonlinearities and additional parasitic effects. Besides interstage matching and in-phase voltage addition, power performances must be evaluated to determine the effectiveness of an additional stage along the stacked architecture. A structured design-flow for dimensioning all the parameters can be

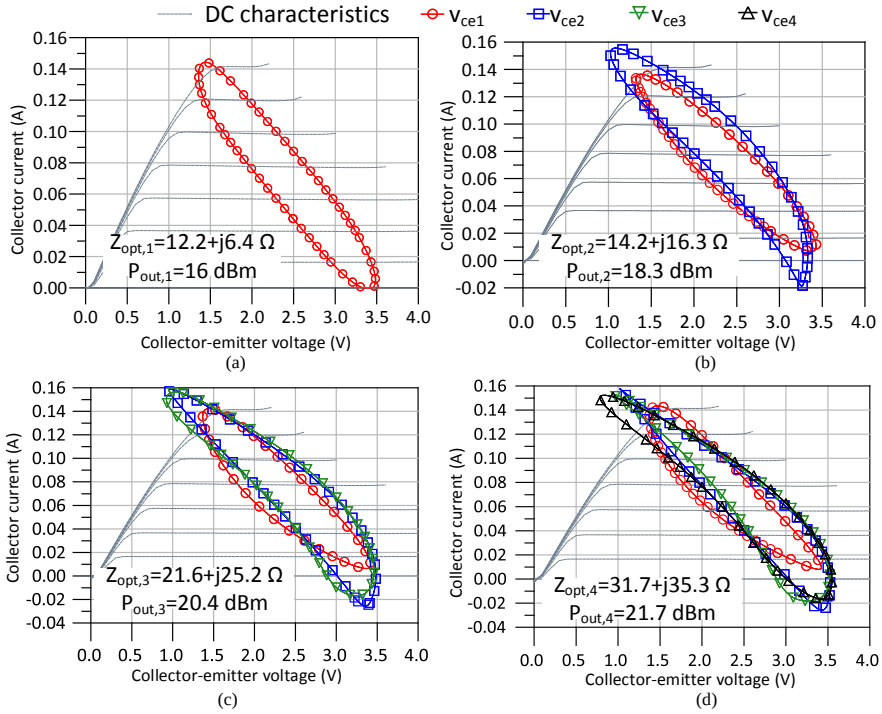


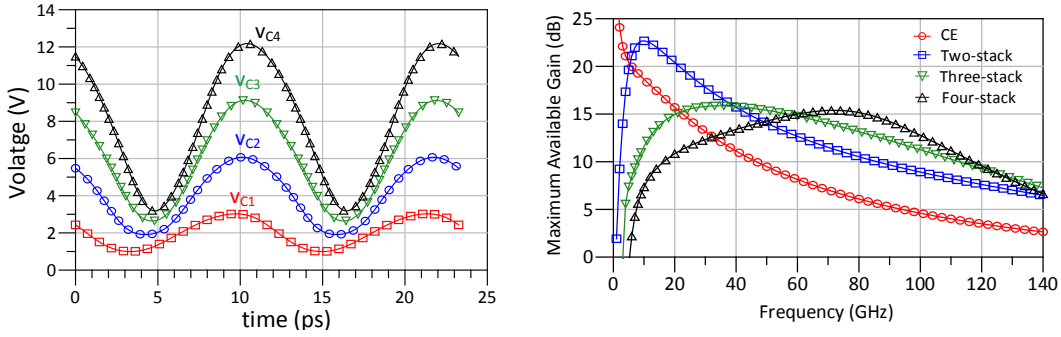
Figure 3.5: Optimized load-cycles for common-emitter (a), two-stacked (b), three-stacked (c) and four-stacked (d) $4 \times 10 \times 0.7\ \mu\text{m}^2$ InP DHBTs transistors at 86 GHz. The input power is kept at $P_{\text{in}} = 10$ dBm in all cases.

synthesized in a few essential points as illustrated in the flow-chart of Figure 3.4.

The initial step is the evaluation of the common-emitter power gain performances and optimum load $Y_{\text{opt},1}$ by means of a load-pull simulation performed on the large-signal model of the selected transistor. At millimeter-waves, in order to achieve acceptable gain and good linearity, Class A bias condition is selected. In this work, four-finger InP DHBT transistors featuring a breakdown voltage $BV_{\text{CEO}} \approx 5$ V and a maximum oscillation frequency $f_{\max} > 350$ GHz have been considered. A modified UCSD HBT model extracted from previous measurements is used in simulations with a bias point $V_{\text{ce}} = 2$ V and $I_{\text{c}} = 60$ mA [49]. The 86-GHz optimum load $Z_{\text{opt},1} = 1/Y_{\text{opt},1}$ and the resulting load cycle for such a transistor in common-emitter configuration is shown in Figure 3.5(a). A first estimation of the circuit parameters of the following common-base stage is then carried out by solving (3.1) and (3.15) in the small-signal analysis with $k = 2$. The found value $Y_{\text{L},2}$ can then be checked in large-signal regime by means of a load-pull simulation performed on the resulting

Table 3.1: Circuit Parameters for the Four-Stacked Transistor

$R_1(\Omega)$	C_1 (fF)	C_2 (fF)	C_3 (fF)
250	300	160	65
C_4 (fF)	$L_{1,2}$ (pH)	$L_{2,3}$ (pH)	$L_{3,4}$ (pH)
40	150	88	75



(a) (b)

Figure 3.6: Resulting collector waveforms of the four-stack transistor at 86 GHz after load cycle optimization (a) and maximum available gain for the common-emitter, two-, three- and four-stacked transistors (b).

two-stacked structure. All the parameters are then optimized so as to obtain maximum voltage and current swings for both devices, as shown in Figure 3.5(b). In this way $Y_{\mathrm{opt},2}$ is obtained and eventually used as the starting point in the design of the following third stage. This procedure can be iterated for the subsequent stages as long as positive incremental power gain is achieved. There will be a value of k for which $P_{\mathrm{out,k}} \leq P_{\mathrm{out,k-1}}$. In this case $n=k-1$ is the maximum number of transistors that can be stacked effectively. In Figure 3.5, the optimized load cycles of the common-emitter, two-stacked, three-stacked and four-stacked transistors operating at the 1-dB compression point at 86 GHz are shown. The power performance improvement of each stage is reported together with the corresponding increase of the load impedance level (or reduction of the load admittance) as predicted in the small-signal analysis.

The values of the circuit elements of the optimized large-signal four-stacked transistor are reported in Table 3.1. Referring to the capacitance values calculated analytically and reported in Figure 3.3(a) for small-signal single-finger devices, one could expect that the values of C_{k} would be just four times higher for four-finger devices. However, when using large-signal models and taking into account the parasitic elements of Figure 2.5, simple linear scaling is not really appropriate and some adjustments have to be made. On the other hand, the principle that C_{k} must decrease with k still holds.

In Figure 3.6(a), the corresponding in-phase voltage waveforms taken at each collector node are reported. The improvements in terms of maximum available gain (MAG) are shown in Figure 3.6(b), where a slight bandwidth reduction can be observed along the stacked architecture as a consequence of the inherently narrow-band reactive tuning of the design approach.

3.2.3 Layout

In Figures 3.7 and 3.8, the schematic and layout views of the common-emitter, two-, three- and four-stacked transistors are shown together with the respective optimized load cycles taken across each device after EM-circuit co-simulations and optimization carried out at 86 GHz on ADS

Momentum by Keysight using SAND transistor models. Resistive feedback networks are used as self-bias and for stabilization [75].

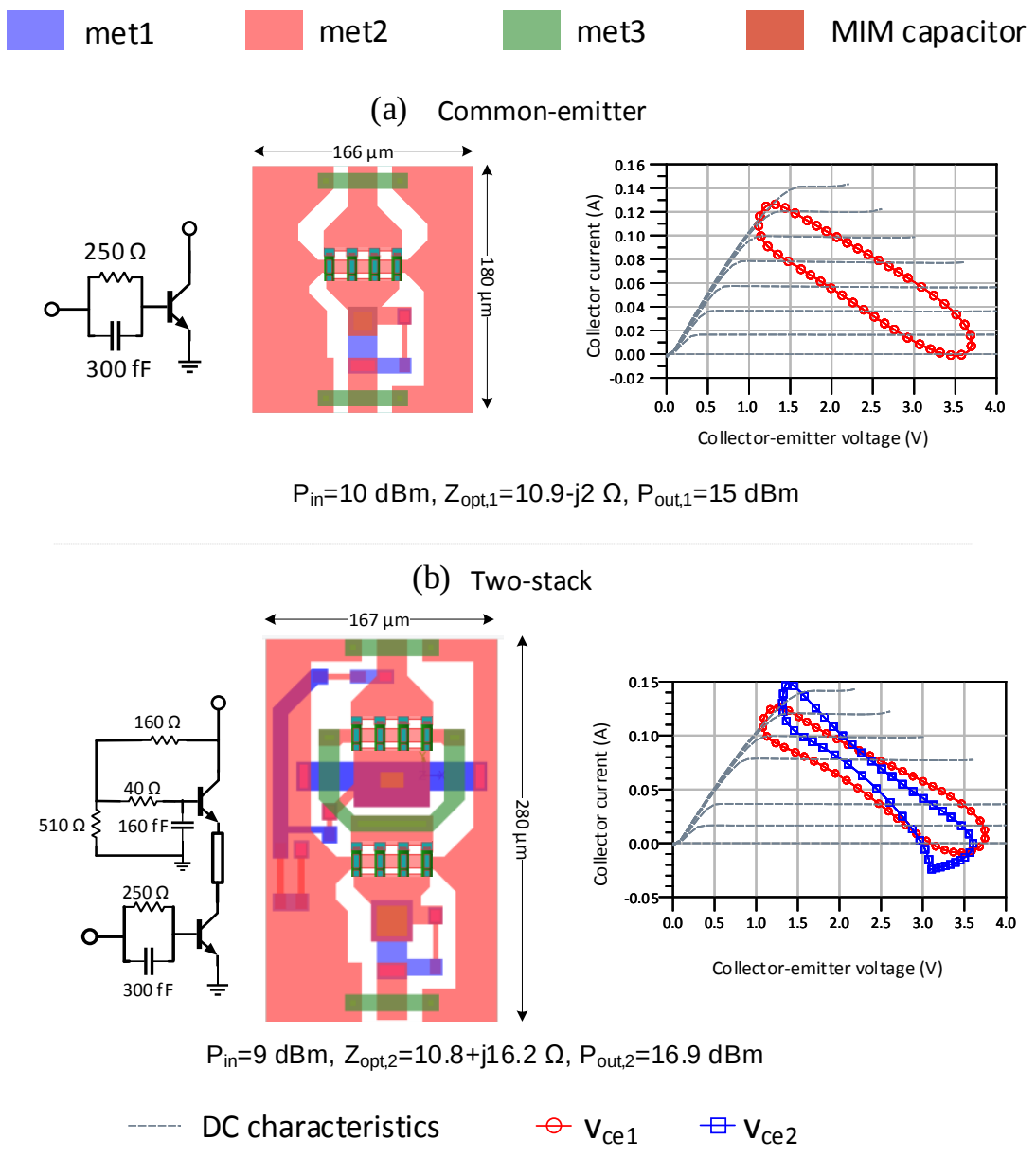


Figure 3.7: Power cells layout of the common-emitter (a) and two-stacked transistors on SAND process with corresponding simulated load cycles after EM-circuit co-simulation at 86 GHz.

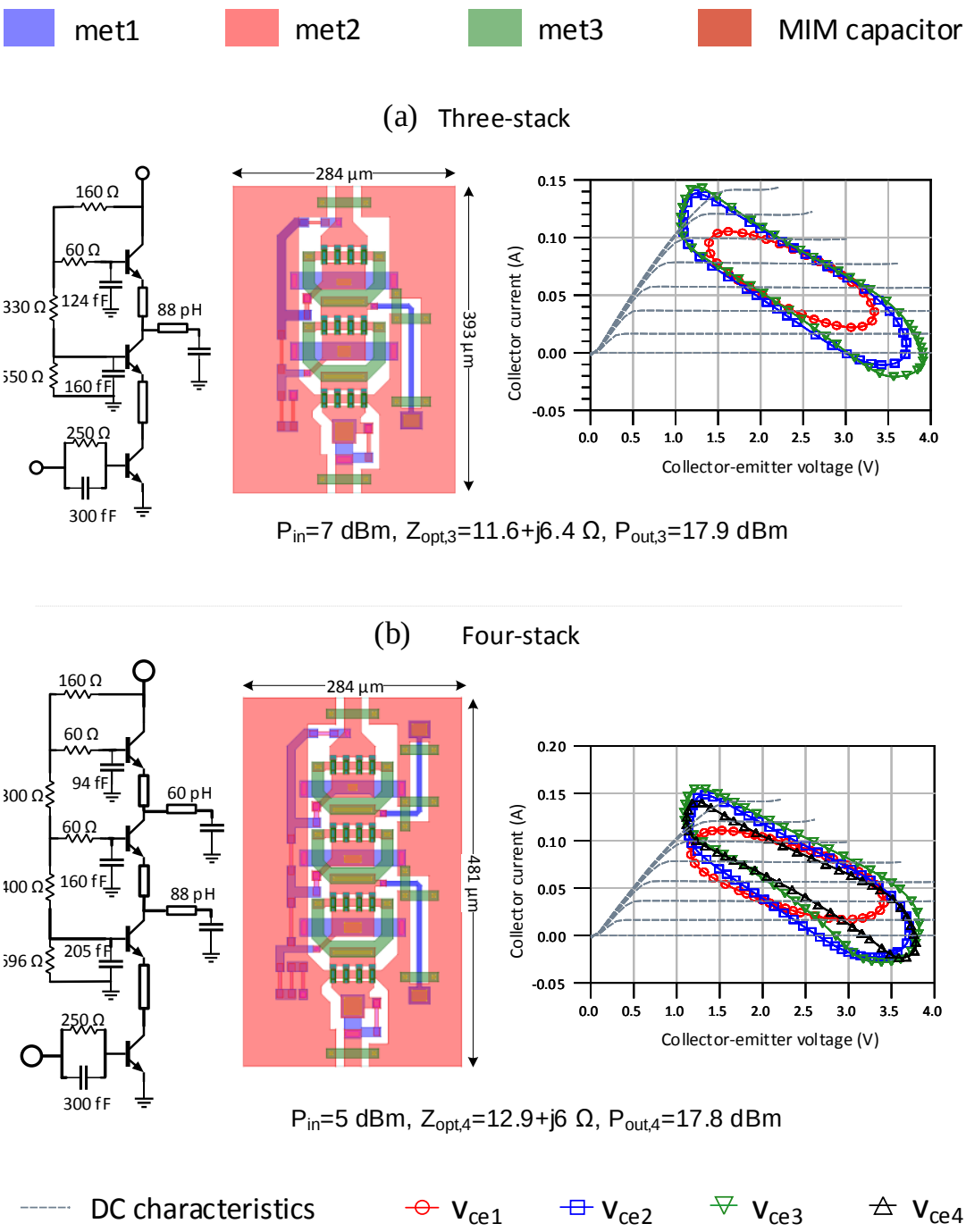
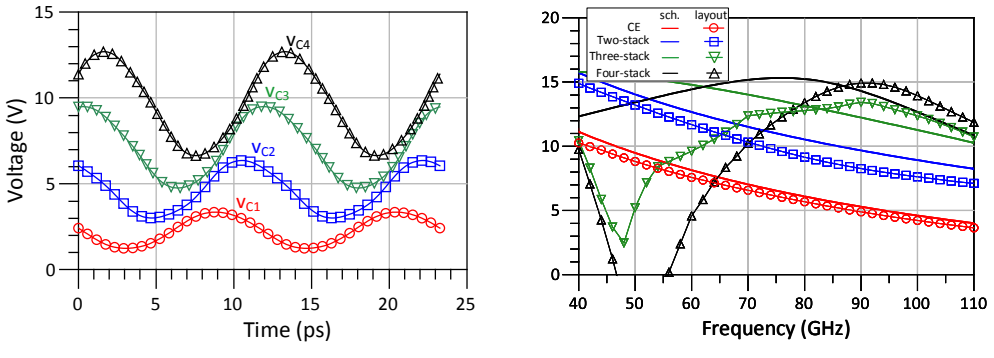


Figure 3.8: Power cells layout of the three-stacked (a) and four-stacked transistors on SAND process with corresponding simulated load cycles after EM-circuit co-simulation at 86 GHz.

As can be seen in Figure 3.7(a), the optimum load of the common-emitter power cell has a small reactive component and a shunt interstage inductor was not necessary in the design of the two-stacked transistor. For the three- and four-stacked transistors of Figure 3.8, the shunt inductors $L_{2,3}$ and $L_{3,4}$ for interstage matching are realized by means of dynamically shorted CPW lines with the central signal trace on *metal1* and ground plane on *metal2*. Given the size constraints, the dc-blocking capacitors are of limited value thus the equivalent LC series cause a resonance effect around 50 GHz. The effective inductance values resulting from these configurations at 86 GHz are $L_{2,3} \approx 88$ pH and $L_{3,4} \approx 60$ pH.

Another extremely important circuit component in the circuit layout of all the stacked-transistors is the finite-length emitter-collector interconnection between adjacent devices. This circuit element, in fact, represents the major limitation for efficient operation as it introduces significant phase misalignment between the collector voltages, as shown in the resulting waveforms of Figure 3.9(a). However, technology-related design rules impose a lower limit on its length and some performance degradation seems unavoidable. In Figures 3.7 and 3.8, the key performance metrics for the four designed power cells are reported. It can be inferred that, while the gain improves considerably with the number of stacked transistors, the power performances are limited by an earlier compression. The three- and four-stacked transistors exhibit comparable output power levels, but compression occurs at lower input power for the latter and, because of the higher bias voltage, it results also in a PAE degradation. Another layout-related effect can be noticed on the values of the optimum load impedances, whose values, differently from the schematic implementation, do not increase substantially with the number of stacked transistors. Some attention has to be drawn also to the effects of layout parasitics on the MAG. Figure 3.9(b) shows the MAG comparison between pure schematic and layout designs. While the degradation for the common-emitter and the two-stacked transistors is due to extra parasitics of the layout implementations, the resonating effect of the shunt interstage CPW lines in the layout of the three- and four-stacked transistors makes their MAG decay considerably around 50 GHz. On the other hand, the series interconnects between the



(a) (b)

Figure 3.9: Collector voltage waveforms at 86 GHz of the four-stacked transistor taking into account layout parasitics (a) and maximum available gain comparison between pure schematic design and taking into account layout parasitics for the four power cells.

devices could be responsible for a small increase of the MAG at higher frequencies, an effect that can be somehow ascribed to an inductive peaking effect.

3.3 Stability Analysis

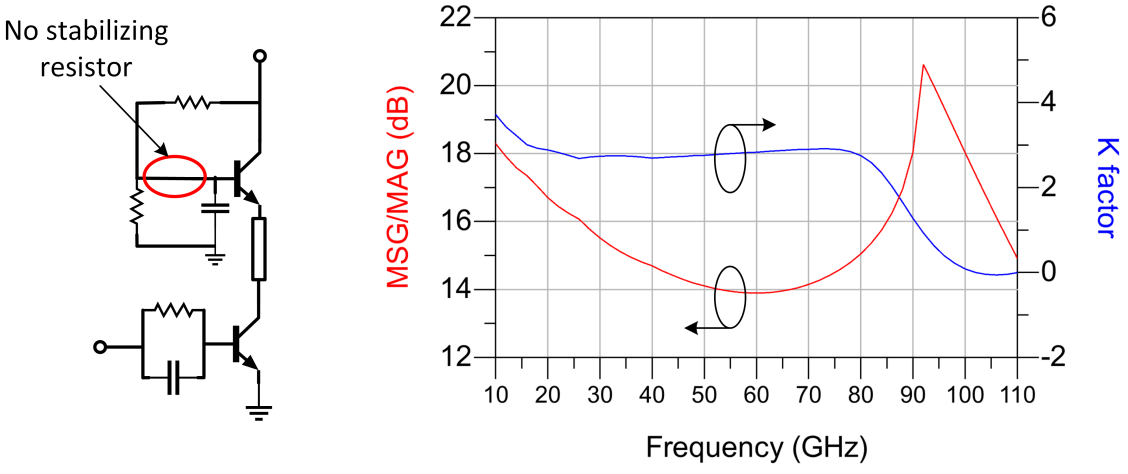
Power amplifiers, like any microwave or mm-wave active circuit, can exhibit undesired spurious oscillations. These are often caused by undetected high gain feedback loops. Careful analysis of all possible source of oscillation must be carried out during the design process. The first and most simple test is based on the small-signal scattering parameters through the K or μ factor. One of the following conditions must be satisfied:

$$\begin{cases} K = \dfrac{1 - |S_{11}|^2 - |S_{22}|^2 - \Delta^2}{2\,|S_{12}S_{21}|} > 1 & \text{(3.16a)} \\ \Delta = |S_{11}S_{22} - S_{12}S_{21}| < 1 & \text{(3.16b)} \end{cases}$$

or

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \qquad (3.17)$$

In making the designed power cells stable, a crucial role is played by the resistances connected to the base terminals. Their action, in fact, can be somehow seen as a damping element against oscillations caused by parasitic inductive interconnects [75]. More rigorously, any equivalent negative resistance is counterbalanced by this circuit component. To further clarify its contribution, some simulation results from a power cell without stabilizing resistor can be informative: in Figure 3.10(a), an example of a two-stacked transistor is shown without stabilizing resistor. As can be seen in Figure3.10(b), the K factor drops below unity around 90 GHz and the power cell becomes potentially unstable, with the MAG increasing up to the maximum stable gain (MSG).



(a) (b)

Figure 3.10: Example of a two-stacked transistor without stabilizing resistor connected to the base. Schematic (a) and simulated MAG/MSG and K factor.

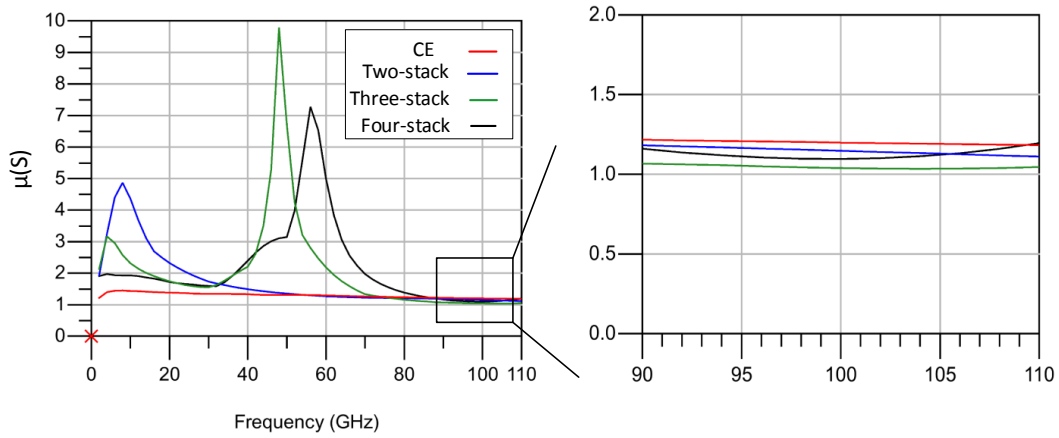


Figure 3.11: μ factor of the stabilized power cells.

Thus, where necessary, a stabilizing resistor is introduced as close as possible to the the base contact, resulting in the power cells of Figures 3.7 and 3.8. Their stability performance are described in the following.

In Figure 3.11, the μ parameter is reported for all the four power cell shown in Figures3.7 and 3.8. It can be seen that it remains higher than one at all frequencies up to 110 GHz. While μ is quite flat for the common-emitter and the two-stacked transistor, it exhibits a peak for the three- and four-stacked transistors due to the gain drop caused by the resonance effect mentioned above. At high frequencies it still remains above unity but with a much smaller margin, as can be seen on the zoomed plot of Figure 3.11.

The μ or K factor tests, however, are not sufficient to guarantee the stability of multiple-stage microwave and mm-wave systems. The pole-zero identification method [76], instead, represents a more complete analysis which allows to tackle hidden oscillations taking place between adjacent stages and it can be used in small-signal and large-signal regimes with various excitation conditions. This method has been applied in the stability analysis of stacked transistors while they are impedance-matched.

3.3.1 Pole-Zero Identification

In Figure 3.12, the schematic representation of the pole-zero identification method applied to the designed power cells is shown, where the current $i_{k,n}(\omega)$ denotes the perturbation applied at the k-th stage of the n-stacked transistor. In simulation, the analysis is performed on the EM-circuit co-simulation setup, so that layout related parasitics are taken into account as well. The transfer functions $H_{k,n}(\omega)$ as:

$$H_{k,n}(j\omega) = Z_{k,n}(j\omega) = \frac{v_{k,n}(j\omega)}{i_{k,n}(j\omega)}, \tag{3.18}$$

where $v_{k,n}$ is the voltage at the node where the perturbation current is applied. The transfer functions $H_{k,n}$ are calculated on Keysight ADS with the aid of the STAN tool by AMCAD. The computed transfer functions are then modeled as a ratio of polynomials whose order is established

based on the desired accuracy of the fitted model. Excessive accuracy, however, can lead to an over-modeling and to the detection of fictitious oscillations which are not existing in reality [77].

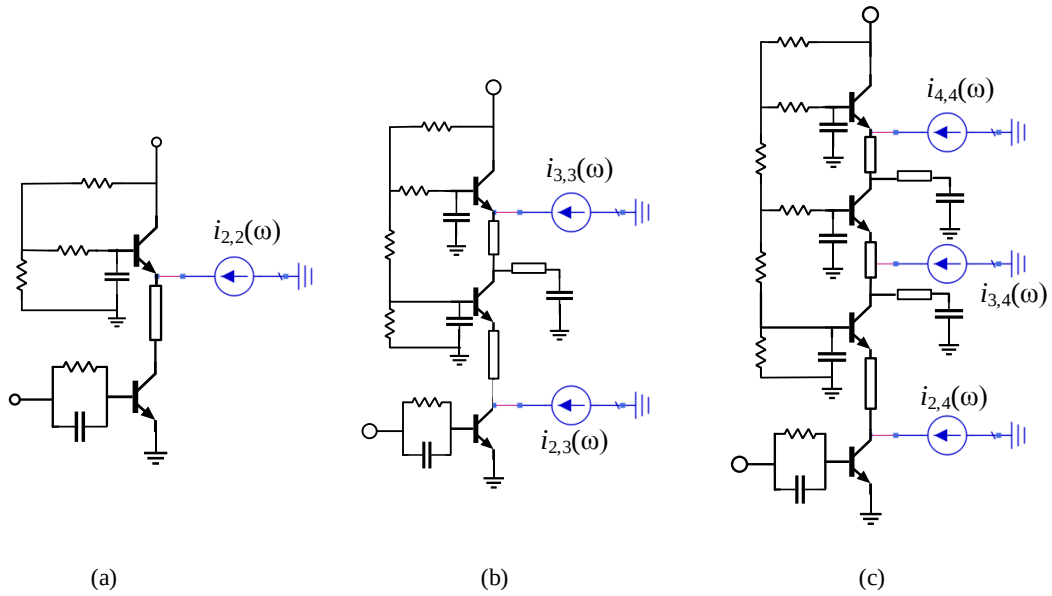


Figure 3.12: Application of the zero-pole identification method by means of the perturbation currents $i_{\mathrm{k,n}}$ to the two-stacked (a) three-stacked (b) and four-stacked transistors.

Two-Stacked Transistor

Figure 3.13 shows the results of the pole-zero identification test carried out in small-signal regime (no drive excitation) on the two-stacked power cell as in Figure 3.12(a). A fourth order has been selected for fitting the transfer function with good accuracy. No poles on the RHP have been detected, indicating stable operation. The pole-zero identification method for the two-stacked transistor has been extended also to the large-signal regime. In this case a mixer-like harmonic balance simulation has been carried out with a drive input power of 10 dBm at 86 GHz. The identification results are shown in Figure 3.14, where a real RHP pole appears. As its imaginary part is zero, however, the computational tool did not provide any warning message for instabilities.

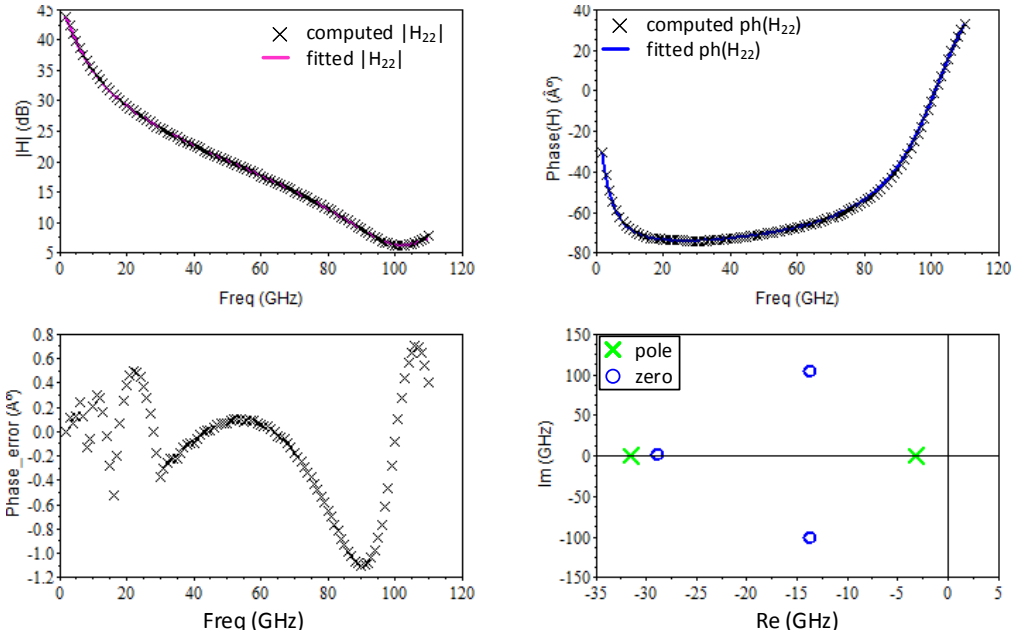


Figure 3.13: Pole-zero identification of the transfer function $H_{2,2}(\omega)$ of fourth order for the two-stacked transistor power cell. No RHP poles are present in this case, indicating stability.

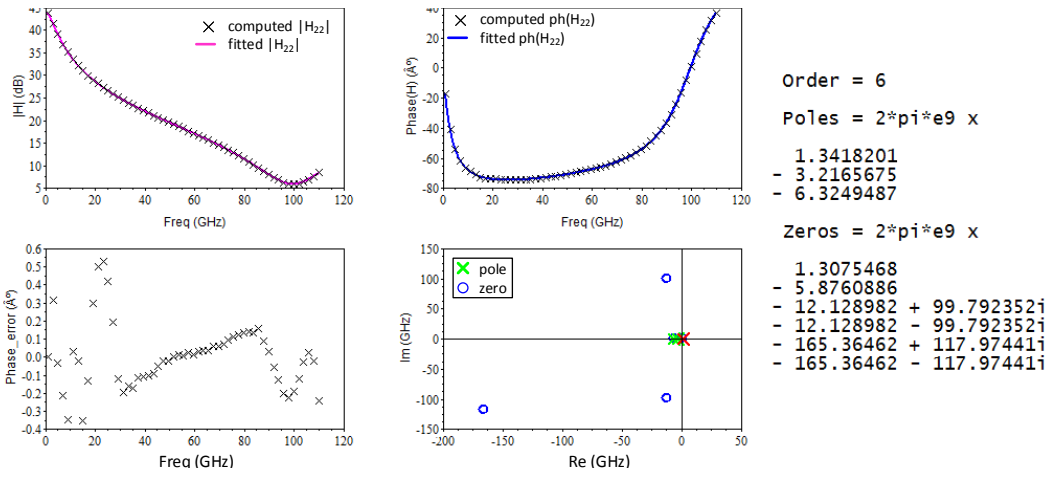


Figure 3.14: Pole-zero identification of the transfer function $H_{2,2}(\omega)$ of sixth order with drive power excitation of 10 dBm at 86 GHz for the two-stacked transistor power cell. A real pole in the RHP is detected in this case but with no warning of instabilities.

Three-Stacked Transistor

The pole-zero identification method performed on the three-stacked power cell has been performed at two distinct access nodes, as shown in Figure 3.12(b). The extraction of the transfer function $H_{2,3}(\omega)$ calculated at the emitter of the second stage is reported in Figure 3.15, where a good fitting with sixth order polynomials is obtained. No poles on the RHP are observed.

The same test on the emitter of the third stage is shown in Figure 3.16. A sixth order polynomial is used for the extraction of the transfer function $H_{3,3}(\omega)$ and no poles on the RHP are observed.

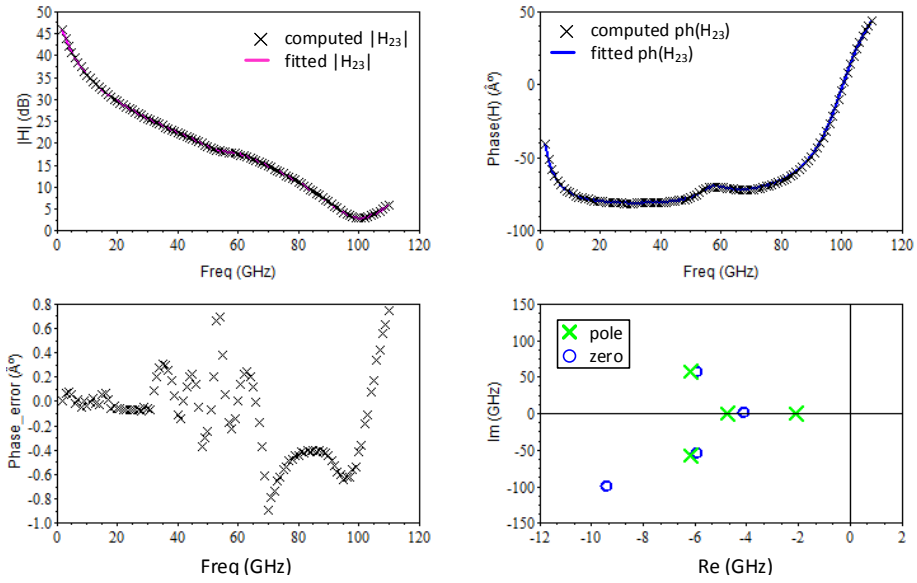


Figure 3.15: Pole-zero identification of the transfer function $H_{2,3}(\omega)$ of sixth order for the three-stacked transistor power cell. No RHP poles are present in this case.

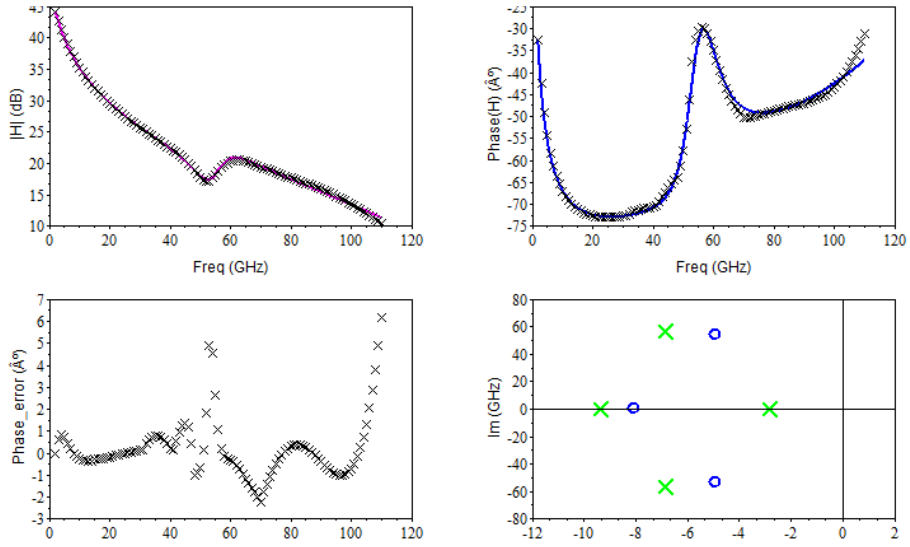


Figure 3.16: Pole-zero identification of the transfer function $H_{3,3}(\omega)$ of sixth order for the three-stacked transistor power cell.

Four-Stacked Transistor

Pole-zero identification results for the four-stacked transistor are shown below. $H_{2,4}(\omega)$, relative to $i_{2,4}(\omega)$ in Figure 3.12(c), presents no poles on the RHP. An initial computation on $H_{3,4}(\omega)$ revealed RHP poles with a possible oscillation at 50 GHz. However, a sub-band analysis in the range 40-60 GHz did not give any indication of instability. The analysis of $H_{4,4}(\omega)$ shows a real pole on the RHP, but as the imaginary part is zero, no oscillations occur.

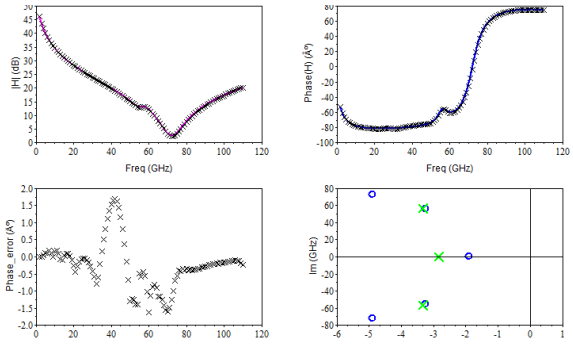


Figure 3.17: Pole-zero identification of the transfer function $H_{2,4}(\omega)$ of sixth order for the four-stacked transistor power cell.

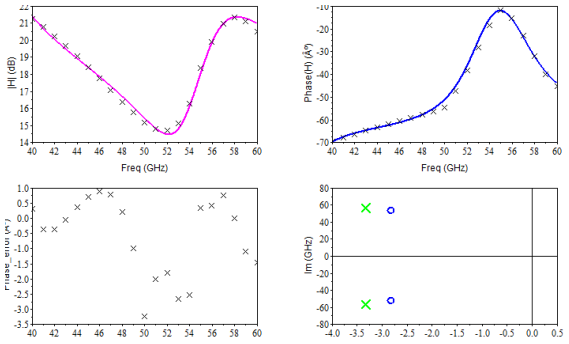


Figure 3.18: Pole-zero identification of the transfer function $H_{3,4}(\omega)$ of sixth order for the four-stacked transistor power cell.

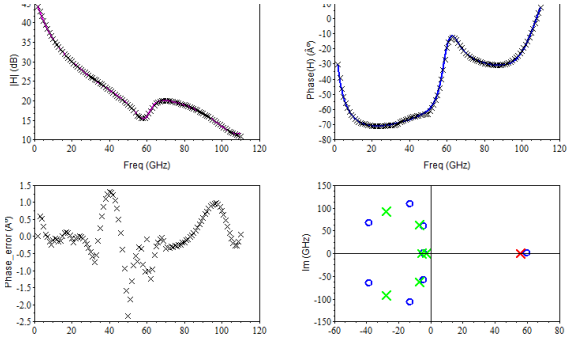


Figure 3.19: Pole-zero identification of the transfer function $H_{4,4}(\omega)$ of eighth order for the four-stacked transistor power cell.

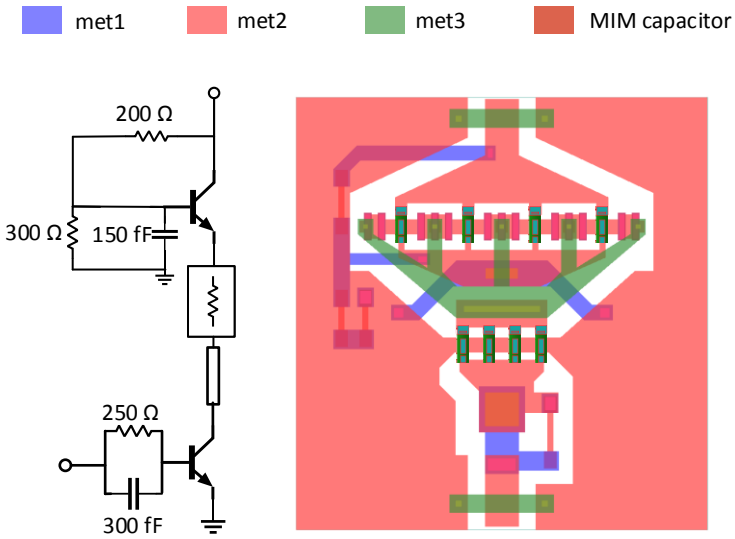


Figure 3.20: Schematic and layout representations of the two-stacked transistor power cell with ballasted common-base.

3.4 Two-Stacked Transistor with Ballasted Common-Base

A further investigation of the stacked-transistor architecture has been carried out by exploiting the power capabilities of the ballasted device presented in the previous chapter 2. In particular, the increased breakdown voltage has been leveraged in this approach. The configuration which proved effective in increasing the output power is a standard common-emitter followed by a ballasted common-base, as shown in Figure 3.20. The connection between the two devices is made of five *met3* sub-connections: two external and three internal plated on top of the ballasting resistors between adjacent fingers. In virtue of the ballasting network and the extended SOA, this power cell is biased with an increased dc voltage of 5.8 V, while the current is kept the same as that of the standard two-stacked transistor.

The response of the power cell taking into account layout parasitic effects through EM-circuit co-simulation are shown in Figure 3.21 and Figure 3.22. In Figure 3.21(a), the maximum voltage and current swings across each transistor are reported for an input power of 10 dBm. The corresponding voltage waveforms taken at the collector nodes are reported in Figure 3.21(b). Note how the overall voltage swing in this case is substantially increased with respect to the standard two-stacked transistor. In fact, the output power in this case is 19.3 dBm (with 10 dBm on input power), which represents a substantial improvement. The optimum load impedance in this case is $Z_{\mathrm{L,opt}} = 6.5 + j4.1\,\Omega$. This rather low value is due to the large area of the transistor and hence to the large parasitic capacitance at its output.

The MAG and the stability parameter μ are reported in Figure 3.22.

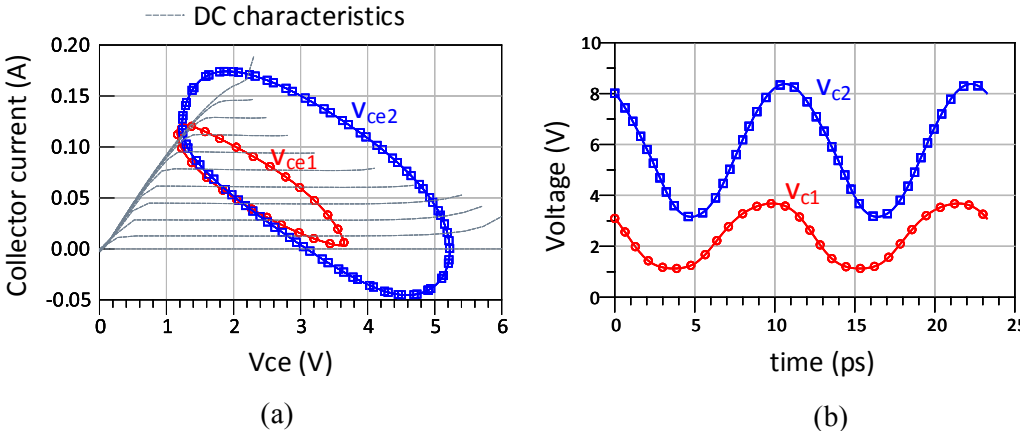


Figure 3.21: Load cycle diagrams (a) and collector voltages (b) of the two-stacked transistor with ballasted common-base. Bias settings: $V_{\mathrm{cc}} = 5.8$ V, $I_{\mathrm{c}} = 60$ mA. The simulated output power is 19.3 dBm with an input power of 10 dBm. the optimum load impedance is $Z_{\mathrm{L,opt}} = 6.5 + j4.1\,\Omega$.

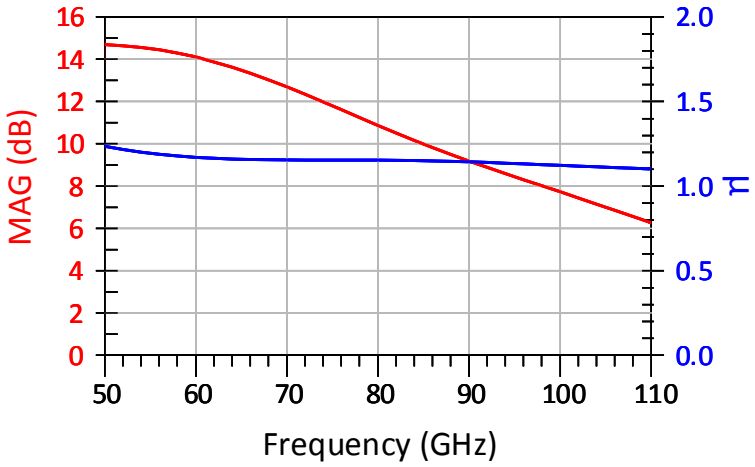


Figure 3.22: Maximum available gain (MAG) and stability parameter μ of the two-stacked transistor with ballasted common-base.

3.5 Summary

It was described in this chapter how the stacked-transistor concept has been applied to InP DHBT technology in an attempt to increase its power performance capabilities at millimeter-wave frequencies. A structured and detailed analysis has been conducted in small- and large-signal regimes, providing a step-by-step guideline for the design procedure. In particular, the fundamental requirements of interstage matching and in-phase voltage addition have been addressed. After a first estimation of the circuit parameters in small-signal operation, the analysis has been extended with the inclusion of large-signal effects, where the the output load cycle of each transistor is examined and optimized for full voltage and current swings. To complete the investigation, the layout is drawn and analyzed through extensive EM simulations. An iterative optimization procedure has

been carried out for reducing unwanted parasitic effects and improving the performances. Limiting factors related to the particular technology have been especially identified in the unavoidable finite-length interconnects between adjacent transistors. In fact, even though they play an important role for interstage matching, these components introduce an undesirable phase misalignment between the collector voltages which translates in earlier compression as the number k of stacked transistors increases. At a certain k, the output power stops increasing and adding further stages would be ineffective. On the other hand, the small-signal gain keeps increasing.

Following the described design procedure, up to four transistors have been connected in series: From a four-finger common-emitter power cell, the design proceeded with two-, three-, and four-stacked transistor power cells. Their simulated performances have been compared in terms of gain and output power. It has been observed that, while the gain keeps increasing with k, the output power at the 1-dB compression point reaches a maximum of about 18 dBm with $k = 3$. Measurement results which are presented in the next chapter confirm this tendency, at least qualitatively.

An additional power cell has been presented in this chapter: a two-stacked transistor where a ballasted device is used as the common-base stage. EM-circuit co-simulation results show how the overall SOA and voltage swing can be significantly increased leading to a higher output power. This is achieved, however, at the expense of a higher bias voltage. The good performances of this power cell are confirmed by experimental results in the next chapter as well.

CHAPTER 4

Implemented Matched Power Cells

The design principles described in Chapter 3 have been verified experimentally for the two-, three- and four-stacked transistors. The relative matched power cells have been implemented and tested in small- and large-signal operations. All the MMIC circuits which are presented in the following were designed specifically using SAND transistor models. Three wafers have been fabricated with the same mask set: two of them were based on the SAND process and one on the SHARC one. Unfortunately, all the test structures on the SAND wafers resulted not functional and experimental verification could not be performed on this process. The SHARC wafer, on the other hand, was functional and measurements were carried out on it. In order to validate the design, *a posteriori* back-simulations of all circuits with SHARC models needed to be performed and this allowed to get a better insight of the potential differences between the two processes. The matching networks have been realized using low-loss coplanar waveguide (CPW) technology with $Z_0 = 50\ \Omega$ of characteristic impedance available in the in-house developed ADS design-kit.

4.1 Two-Stacked Transistor Power Cell

Figure 4.1(a) and (b) show the schematic and chip microphotograph, respectively, of the matched two-stacked transistor power cell. The bias voltages V_{cc} and V_{bb} are 4.9 V and 1.7 V, respectively, resulting in a total current of 80 mA, including the current flowing in the resistive feedback network. The bypass capacitors $C_1 = 500$ fF provide dynamic shorts at the operating frequencies, while the series R_2-C_2 (20 Ω-2 pF) helps to attenuate eventual low frequency oscillations. To fit the entire circuit into the standard MMIC size of $1.2 \times 1.5\ \mathrm{mm}^2$, the input matching network has been realized as a T-shape.

Figure 4.2 shows the comparison between simulated and measured S-parameters of the matched two-stacked power cell. As can be seen, the original design targeted for the SAND process exhibits far better performances than the SHARC one. The simulated peak $|S_{21}|$ in SAND process is 11.1 dB at 86 GHz, while the measured $|S_{21}|$ on SHARC drops below 5 dB at frequencies higher than 80 GHz. Overall, backward simulations with SHARC models agree quite well with measurements, except for a slightly lower gain between 70 and 90 GHz.

Power sweep measurements are reported in Figure 4.3 at four different frequencies from

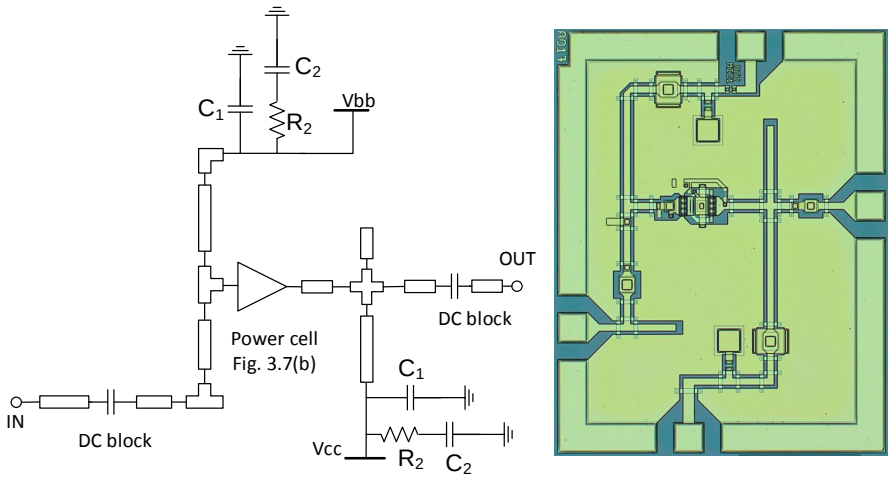


Figure 4.1: Schematic view (a) and chip microphotograph (b) of the matched two-stacked transistor power cell. The chip size is $1.2 \times 1.5\,\mu\text{m}^2$.

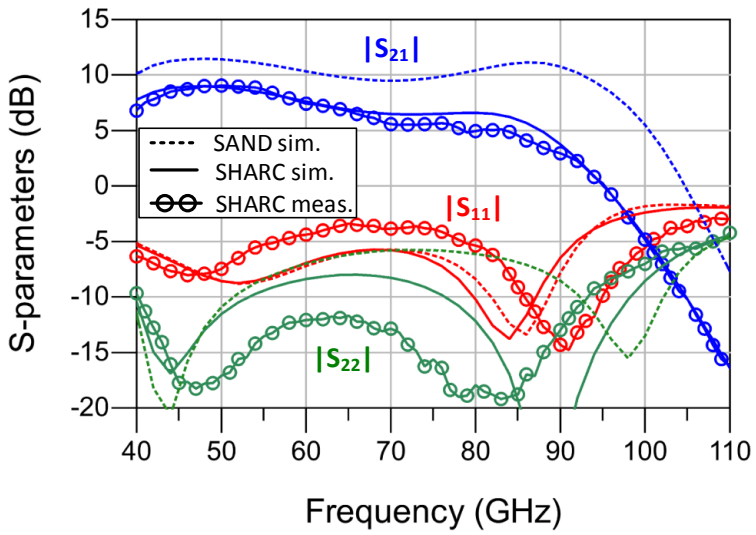


Figure 4.2: Measured and simulated S-parameters of the matched two-stacked transistor power cell.

75 GHz to 84 GHz and compared to simulations (the details of the measurement setup are described in Appendix A). As can be seen, there is good agreement between SHARC simulation and measurements for all four cases, even though measurements seem quite optimistic if compared to S-parameters measurements. This little contradiction can come from a small uncertainty in the calibration of the large-signal measurement setup. Qualitatively, however, these measurements are consistent with S-parameters. Measured large-signal results seem to exhibit a slightly earlier

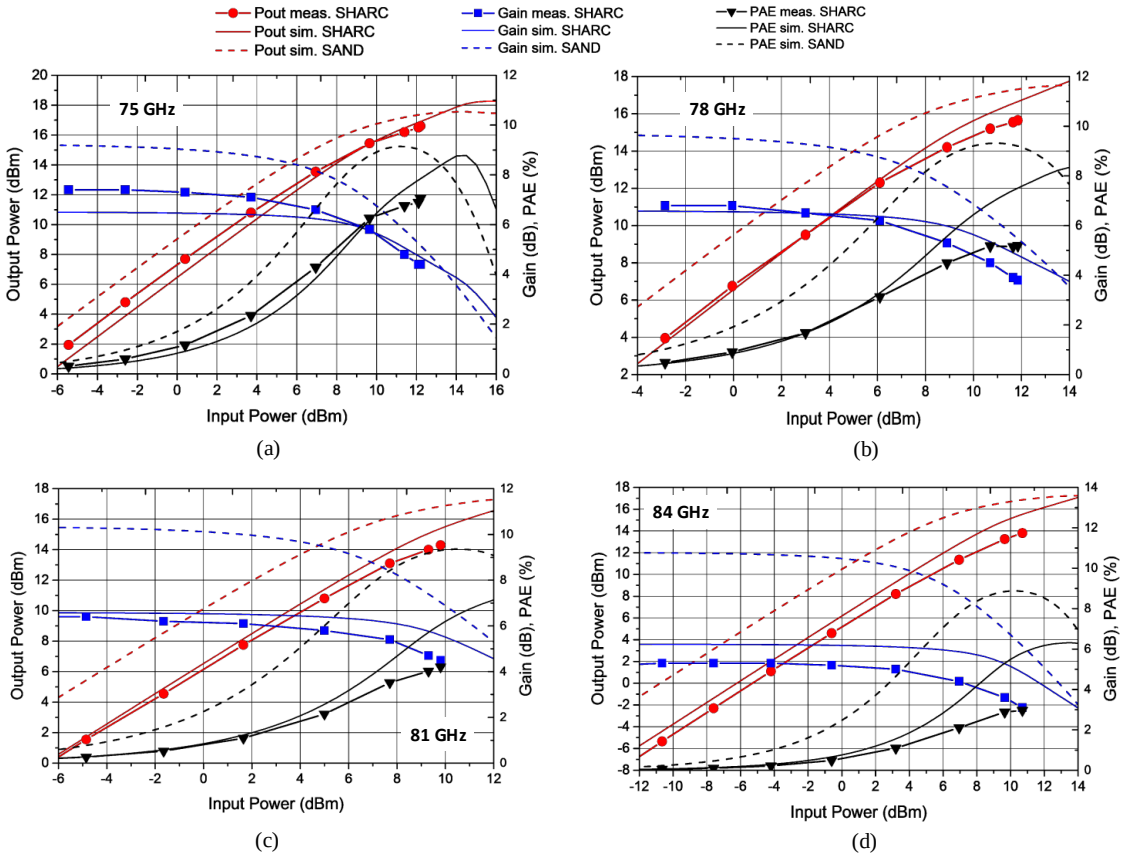


Figure 4.3: Measured and simulated power sweep of the matched two-stacked transistor power cell.

Table 4.1: Summary of the measured large-signal performances of the two-stacked transistor power cell.

freq (GHz)	Gain (dB)	Pout,1dB (dBm)	Pmax (dBm)	peak PAE (%)
75	7.4	14	16.6	7.1
78	6.8	13	15.7	5.2
81	6.4	13.1	14.3	4.2
84	5.2	11.5	13.8	3

compression due to some accuracy issues of large-signal modeling. SAND simulations predict a substantially higher small signal gain but the saturated output power is comparable with the SHARC process. This is not surprising: The lower breakdown voltage of the SHARC process is compensated by its lower knee voltage, so comparable maximum voltage swing is achieved for the two processes. The overall good agreement between measurements and back-simulations is in some way a first clear proof of the good accuracy of device and circuit modeling carried out in this work.

Table 4.1 summarizes the measured large-signal performances of the fabricated matched two-stacked power cell. It should be noted that the values of $P_{\max}$ in the table are the maximum level of

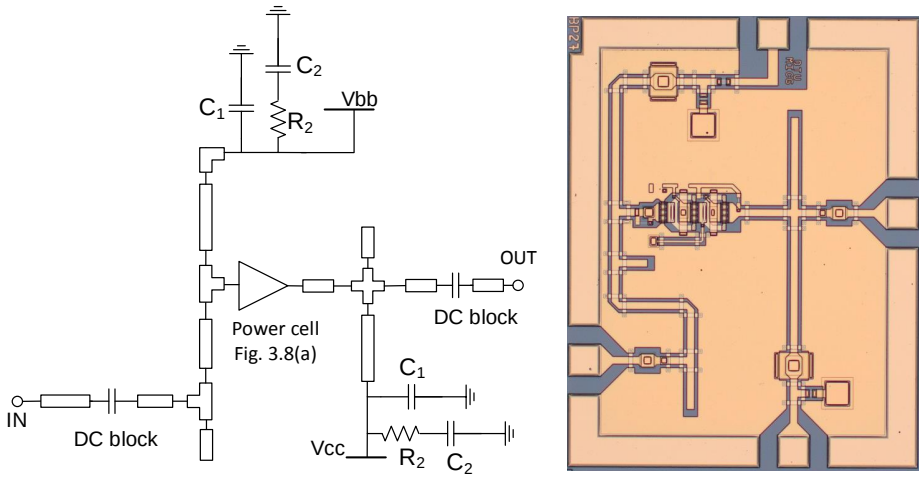
output power obtained with the available power source (see Appendix A). The power cell, however does not reach full saturation and a higher output power could be expected if more input power were available.

4.2 Three-Stacked Transistor Power Cell

Figure 4.4(a) and (b) show the schematic and chip microphotograph, respectively, of the matched three-stacked transistor power cell. The bias voltages in this case are $V_{\rm cc} = 6$ V and $V_{\rm bb} = 1.7$ V. The resistive feedback network has been better optimized with respect to the two-stacked transistor so as to absorb less dc power. The total collector current is 70 mA. As the three-stacked power cell is slightly bigger in size and must be accommodated in the same standard chip size of $1.2 \times 1.5\ \mathrm{mm}^2$, the input matching network features a meandering structure, which eventually introduced extra losses.

Measured and simulated S-parameters are reported in Figure 4.5. The measured peak $|S_{21}|$ is 8.6 dB and occurs at 80 GHz. A 15-GHz 3-dB bandwidth is obtained in the range 70-85 GHz and the input return loss is better than 10 dB from 77 GHz to 84 GHz. Back-simulations on SHARC models seem to reflect measured performances, except for a frequency shift of approximately 5 GHz. Most likely, in the realized MMIC, the input matching network with many bending structures could feature an excess capacitive loading not properly taken into account in simulations. The original design on SAND process is perfectly matched at 86 GHz with a peak $|S_{21}|$ of 13.3 dB at 90 GHz.

In Figure 4.6, large signal measurements and simulations are reported at four different frequencies from 75 GHz to 84 GHz and in Table 4.2, the main performance metrics are summarized.



(a) (b)

Figure 4.4: Schematic (a) and chip microphotograph (b) of the matched three-stacked transistor power cell. The chip size is $1.2 \times 1.5\,\mathrm{mm}^2$.

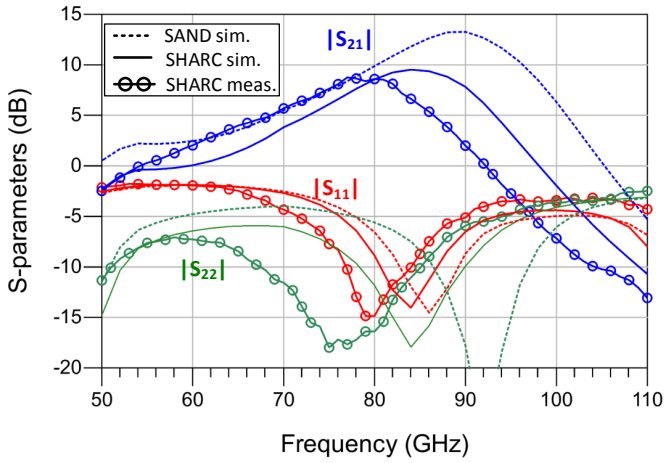


Figure 4.5: Measured and simulated S-parameters of the matched three-stacked transistor power cell.

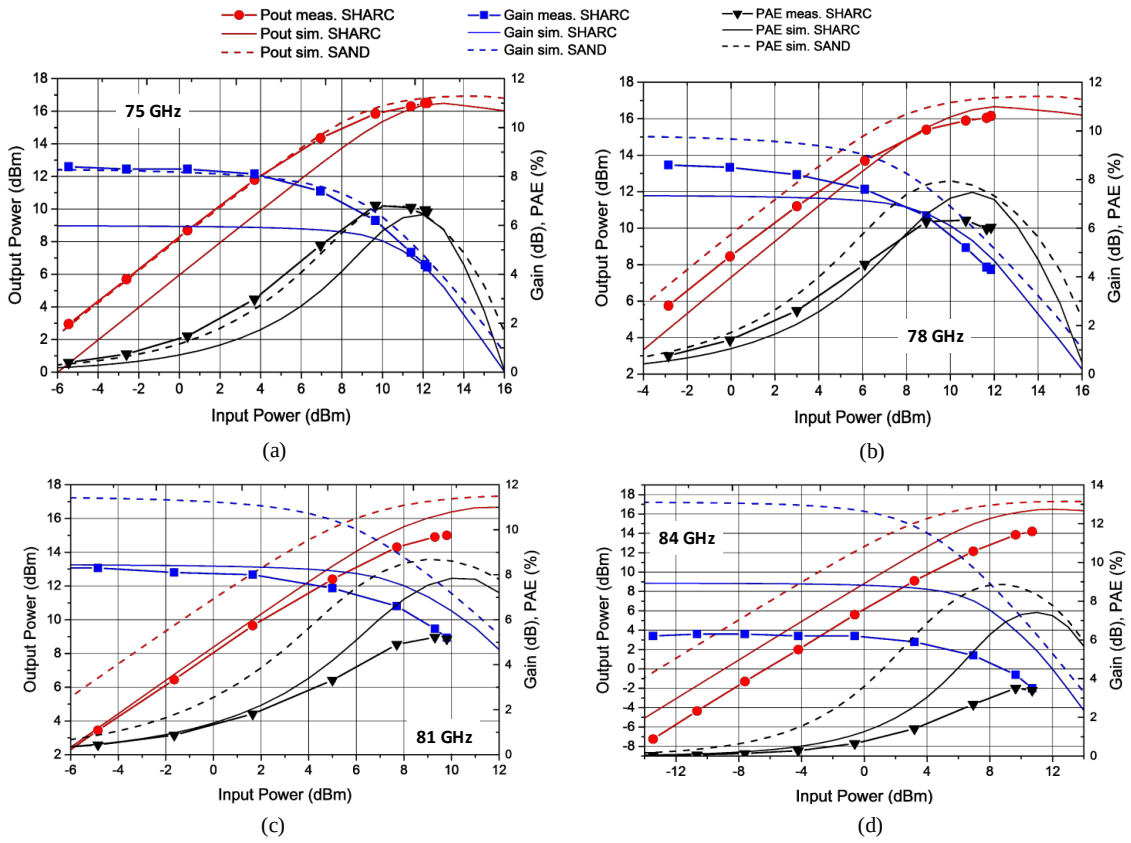


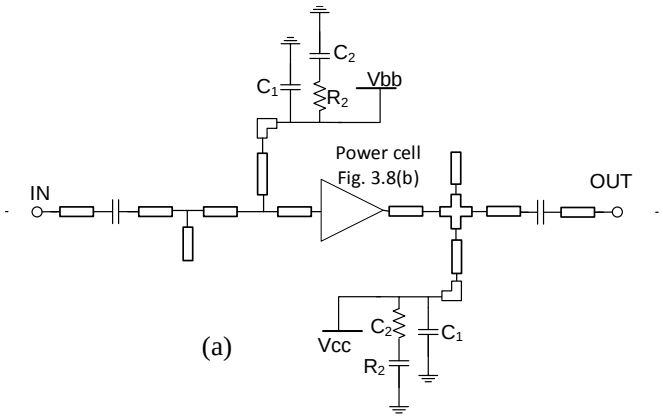
Figure 4.6: Measured and simulated power sweep of the matched three-stacked transistor power cell.

Table 4.2: Summary of the measured large-signal performances of the three-stacked transistor power cell.

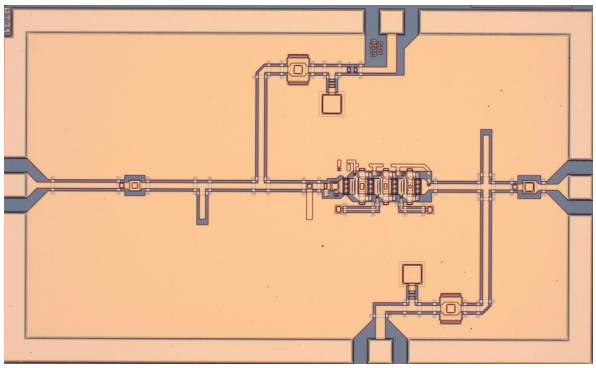
freq (GHz)	Gain (dB)	Pout,1dB (dBm)	Pmax (dBm)	peak PAE (%)
75	8.4	14.4	16.5	6.8
78	8.6	13.7	16.2	6.3
81	8.3	12.5	15	5.2
84	6.2	12.2	14.2	3.5

4.3 Four-Stacked Transistor Power Cell

For the realization of the four-stacked transistor matched power cell (Figure 4.7), the requirements on the chip size were less stringent, so a straight input matching network could be realized. The MMIC size in this case is $2.4 \times 1.5\ \mathrm{mm}^2$. The bias voltage is $V_{\mathrm{cc}} = 8$ V and the collector current $I_{\mathrm{C}} = 70$ mA. The measured and simulated S-parameters are reported in Figure 4.8. The measured peak $|S_{21}|$ is 11.4 dB at 83 GHz. A 12-GHz 3-dB bandwidth is obtained from 74 GHz to 86 GHz and the input return loss is better than 10 dB from 78 GHz to 88 GHz. A good agreement with SHARC back-simulations is observed. SAND simulations exhibit a peak $|S_{21}|$ of 14.8 dB at 88 GHz and, like in the previous cases, are slightly shifted upward in frequency.



(a)



(b)

Figure 4.7: Schematic (a) and chip microphotograph (b) of the matched four-stacked transistor power cell. The chip size is $2.4 \times 1.5\,\mathrm{mm}^2$.

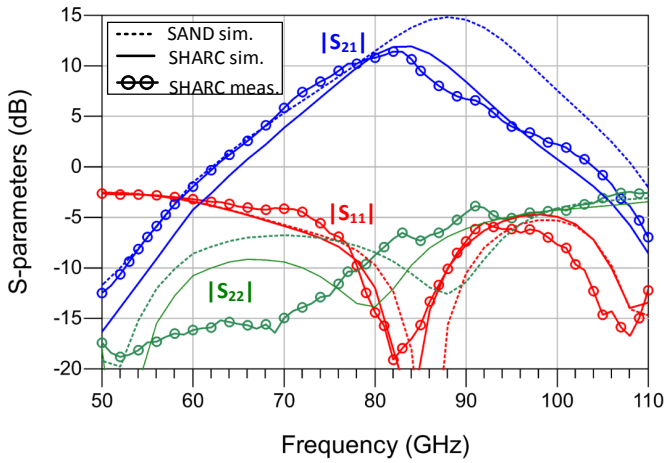


Figure 4.8: Measured and simulated S-parameters of the matched four-stacked transistor power cell.

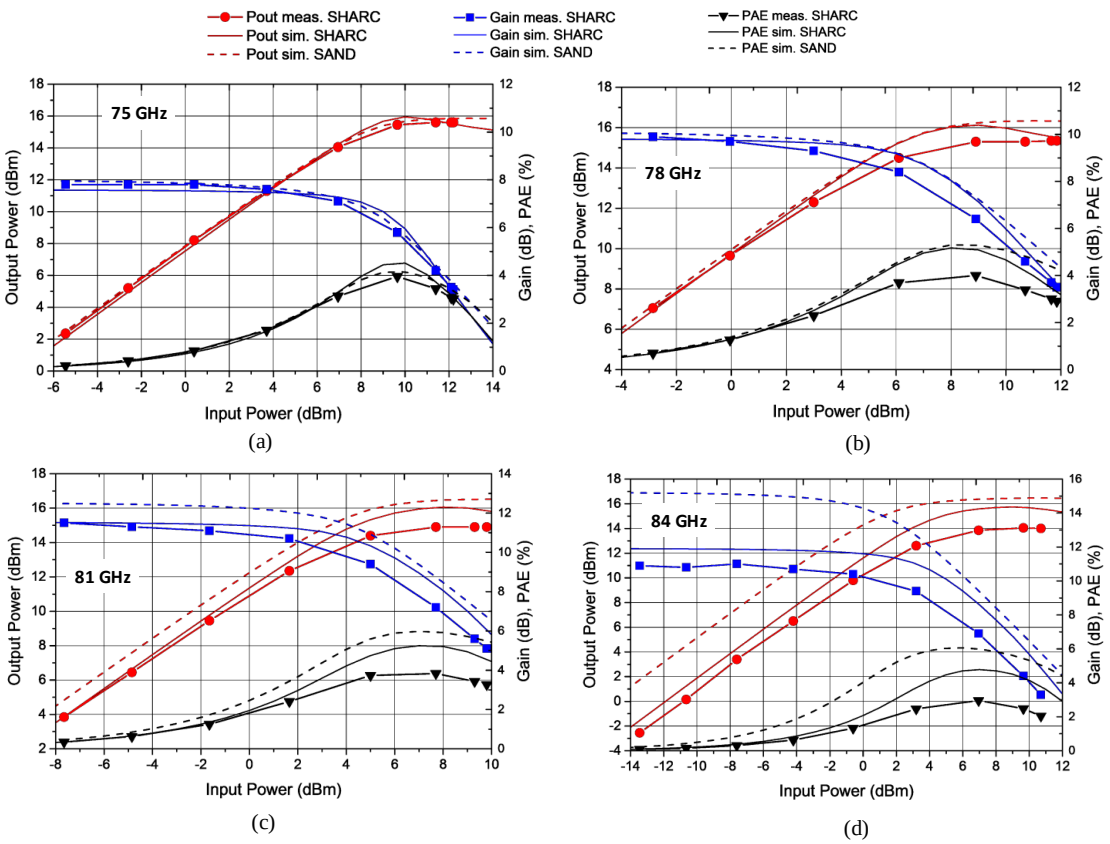


Figure 4.9: Measured and simulated power sweeps of the matched four-stacked transistor power cell.

Table 4.3: Summary of the measured large-signal performances of the four-stacked transistor power cell.

freq (GHz)	Gain (dB)	Pout,1dB (dBm)	Pmax (dBm)	peak PAE (%)
75	7.8	14.7	15.6	4
78	9.9	13.2	15.4	4
81	11.5	12.5	14.9	3.8
84	10.9	11	14	3

In Figure 4.9, large signal measurements and simulations are reported at four different frequencies from 75 GHz to 84 GHz and in Table 4.2, the main performance metrics are summarized.

It is interesting to compare the performances of the three MMIC power cells examining the results reported so far. The different power performance characteristics of the three matched power cells can be better evaluated by comparing their broadband frequency response under large signal excitation. In Figure 4.10, the measured output power of the three circuits are compared as function of frequency, with the input power being the maximum available one shown in Appendix A, for which all these circuits operate under compression.

Based on the analysis of the previous chapter and the experimental results reported here, we can conclude that, in this InP DHBT technology, the stacking architecture can be beneficial up to three stages. The main limitations arise from layout parasitics which can be limited only partially due to the design rules related to the process.

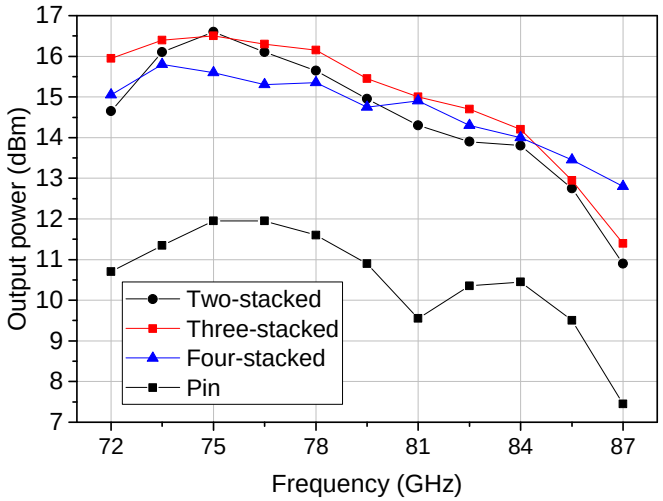
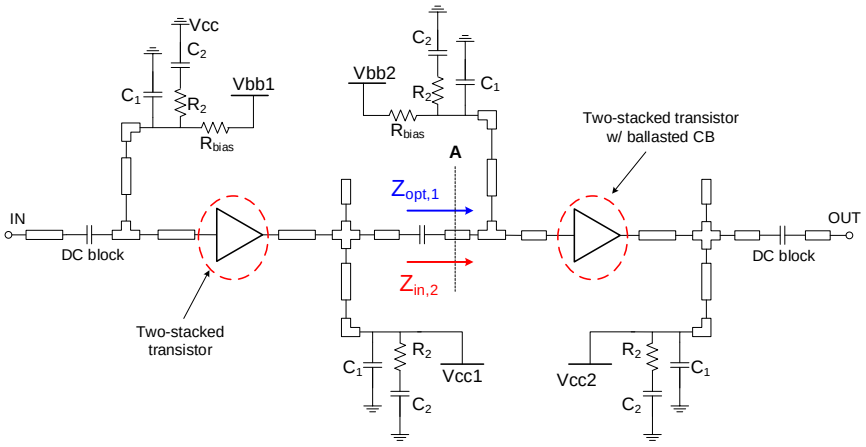


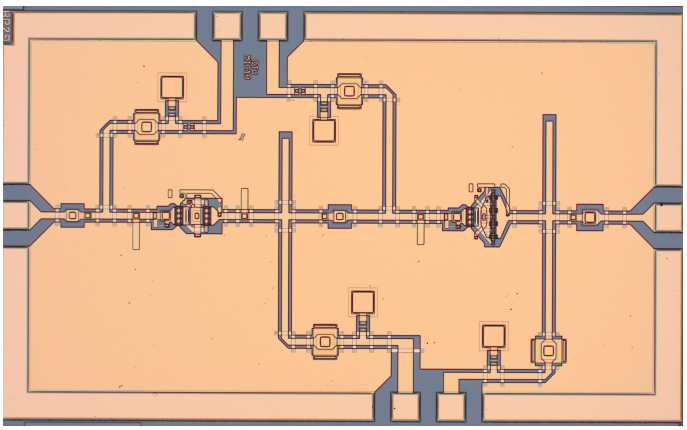
Figure 4.10: Comparison of the broadband maximum output power for the two-, three and four-stacked transistor power cells.

4.4 Two-Stage Two-Stacked Power Amplifier with Output Balasted Common-Base

The previously described two-stacked transistor with ballasted common-base is used in this design as the output stage of a two-stage power amplifier. To counterbalance the limited gain of the ballasted transistor, a driver stage is added in this case, which is the standard two-stacked transistor. In Figure 4.11(a) and Figure 4.11(b), the schematic representation and the chip microphotograph are shown, respectively. The bias voltages of the first and second stages are set to $V_{\mathrm{cc1}} = 4$ V and $V_{\mathrm{cc2}} = 5.9$ V. The current levels of the two stages are $I_{\mathrm{cc1}} = 70$ mA and $I_{\mathrm{cc1}} = 80$ mA, respectively. Also in this case, matching networks are realized by means of 50-Ω CPW. In order to avoid undesired reflections and gain reductions, special care is devoted to the design of the interstage matching network between the two stages. In particular, lines and components have been dimensioned in such a way that, at plane A in the schematic, the input impedance of the



(a)



(b)

Figure 4.11: Schematic (a) and chip microphotograph (b) of the Two-stage power amplifier with ballasted common-base power stage. The chip size is $2.4 \times 1.5\,\mathrm{mm}^2$.

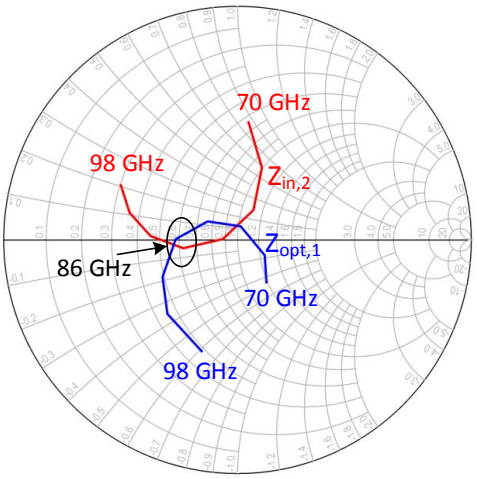


Figure 4.12: Plots for the design of the interstage matching network of the two-stage amplifier: Optimum load impedance of the driver stage and input impedance of the second stage as functions of frequency.

second stage is equal to the optimum load impedance of the driver stage, at least at the frequency of interest, i.e. 86 GHz. This can be seen on the Smith chart of Figure 4.12, where the two quantities are reported as functions of frequency in the range 70-98 GHz and come very close at 86 GHz.

S-parameters measurements and simulations are reported in Figure 4.13. As always, simulation results from the two processes SHARC and SAND can be compared, while only SHARC measurements are available. The measured gain is higher than 10 dB from 30 GHz to 85 GHz and the peak $|S_{21}|$ is 13.9 dB at 71 GHz. The original design on SAND process is centered at 85 GHz, while back-simulation on SHARC result centered at 79 GHz. A further downshift to 77 GHz resulted from SHARC measurements. The simulated peak $|S_{21}|$ in SAND occurs at 81 GHz and is 20.2 dB.

Large-signal measurements are reported in Figure 4.14 from 75 to 84 GHz. During large-signal measurements, the driver stage could not be biased at the nominal voltage because of reliability issues: With V_{CC1} higher than 3.5 V, the circuit burned and a safer bias of 3 V was selected on another site of the wafer. A summary of the performances are reported in Table 4.4.

Table 4.4: Summary of the measured large-signal performances of the two-stage amplifier with ballasted output common-base.

freq (GHz)	Gain (dB)	Pout,1dB (dBm)	Pmax (dBm)	peak PAE (%)
75	12.2	11.6	17.3	5.3
78	11.9	12	16.9	4.8
81	12.1	10	15.6	3.9
84	9.7	8.1	14.2	2.3

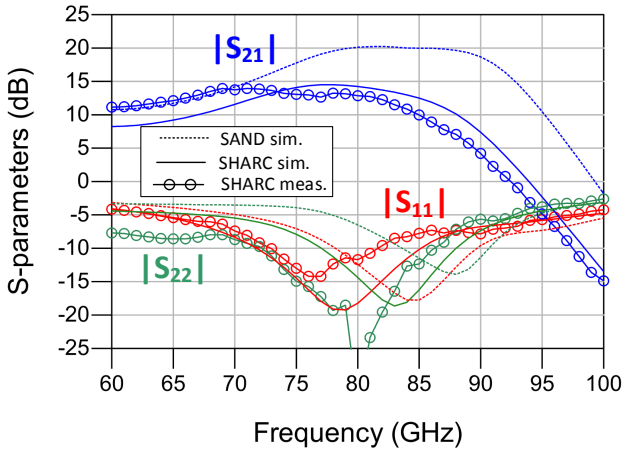


Figure 4.13: Simulated and measured S-parameters of the Two-Stage Power Amplifier with Ballasted Common-Base Power Stage.

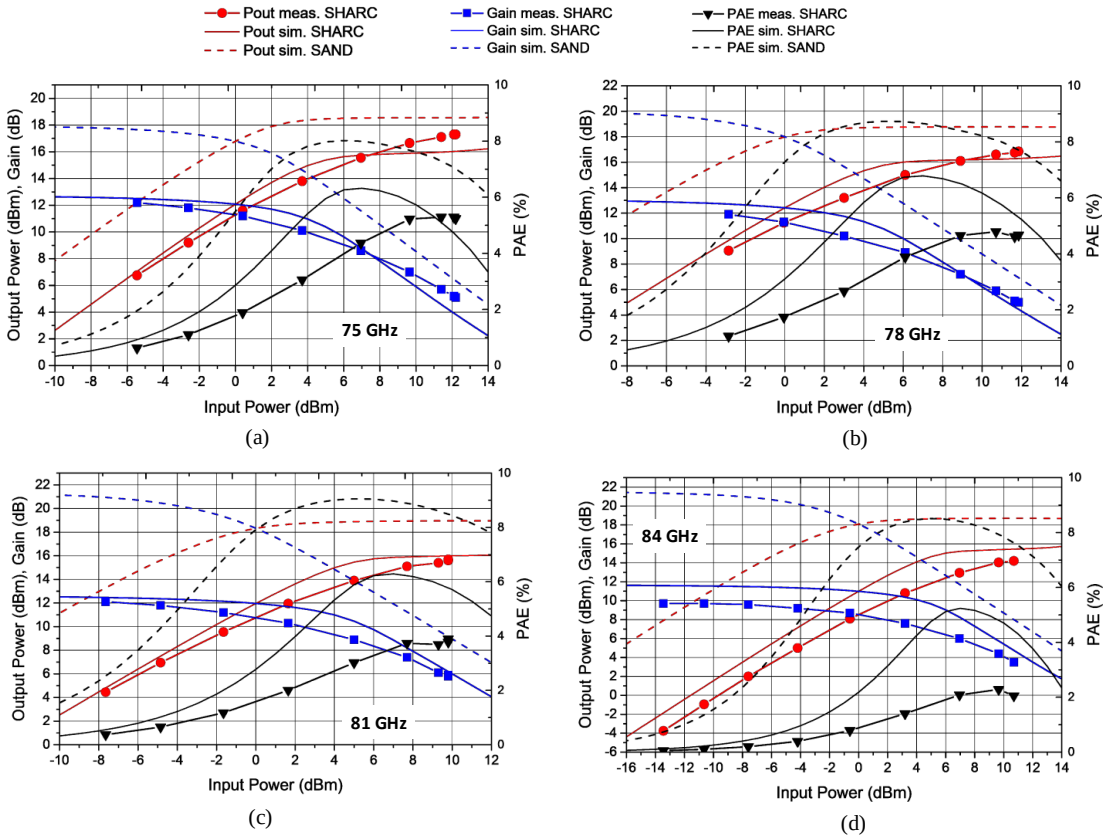


Figure 4.14: Measured and simulated power sweep of the two-stage power amplifier with ballasted common-base.

4.5 Summary

This chapter reports the experimental results obtained from the fabricated MMIC matched power cells. After a description of the circuit topologies with their matching and bias networks, the measured performances are reported for the two-, three-, and four-stacked transistors implemented on a SHARC wafer. The original simulations carried out on SAND models are reported as well for better understanding the performance differences between the two processes. In order to validate the design, back-simulations performed on SHARC models are compared against measurements. Except for a small frequency downshift, a good agreement can be observed in all cases.

For the two-stacked transistor, the measured small-signal gain $|S_{21}|$ is approximately 5 dB around 80 GHz. For the three- and four-stacked ones, 8.6 dB and 11.4 dB are obtained, respectively. Such a significant improvement in the gain performances is not paralleled by an equivalent output power enhancement, as was also predicted in the analysis of the previous chapter. For instance, at 81 GHz, the maximum output power is around 15 dBm in all three cases, with a difference between them not larger than 1 dB. This also means that an earlier compression occurs with higher stacking orders. Except for the gain, the best performances in terms of output power and PAE are obtained with the three-stacked transistor, which is thus believed to be the best compromise.

The original SAND designs, centered at 86 GHz, exhibit in all cases a simulated small-signal gain of several dB's higher than SHARC designs do, confirming its better performances for analog applications. When it comes to power performance, however, an early compression is observed and the saturated output power becomes comparable to the one obtained with the SHARC process. This can be somehow attributed to the higher collector layer of the SAND process which entails, among other things, a higher collector resistance and hence a higher knee voltage, so that the maximum voltage swing does not fully benefit from the higher voltage breakdown BV_{ceo}.

The implementation and the experimental results of another MMIC design have been reported in this chapter. It is a two-stage power amplifier featuring a two-stacked transistor with ballasted common-base in the output stage and a standard two-stacked transistor in the driver stage. As was predicted in the analysis, a higher bias voltage (5.9 V against 4 V) can be easily sustained with this configuration and a higher output power could be achieved. At 81 GHz, for instance, 15.6 dBm was obtained while not fully saturated. A higher output power could be expected if a higher input power were available. Thanks to the two-stage implementation, a considerable small-signal gain of 13.9 dB at 71 GHz has been reported. Also in this case, a good agreement between measurements and back-simulations can be observed.

CHAPTER 5

Implemented Power Amplifiers

Besides series voltage addition realized by the stacked-transistor topology, parallel combining has been used to further increase the transmitted power. In this chapter, several MMIC power amplifiers are presented, where the basic power cells of Chapter 3 are combined on chip in various forms to achieve high output power and/or high gain. Thanks to its simplicity in the design approach, the corporate power divider/combiner topology has been selected in all the circuit designs. The general approach in this investigation was to design and test a parallel-combined power stage and successively adding a driver stage to increase the gain. Four-way and eight-way parallel combined structures are used as output power stages and two-way combined structures are mostly used as driver stages.

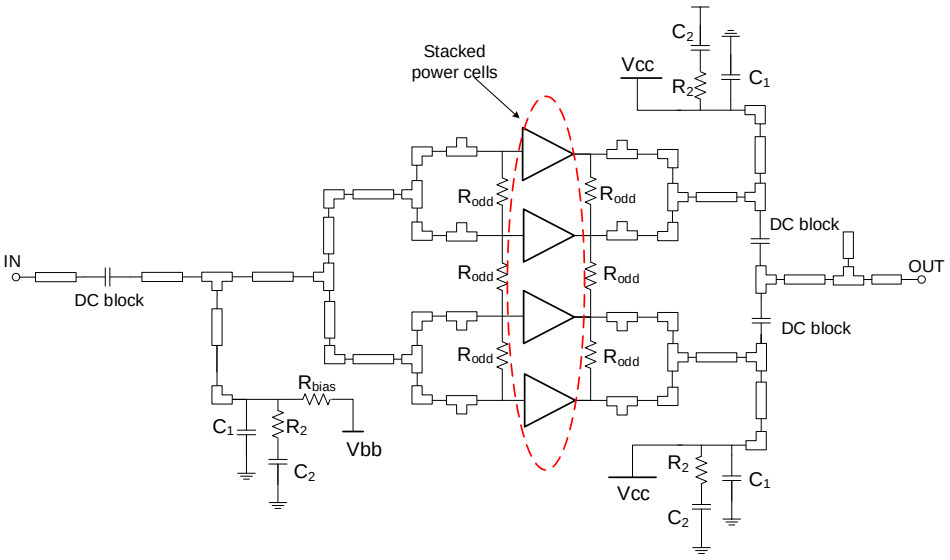


Figure 5.1: Schematic representation of a four-way combined power stage.

5.1 Four-Way Combined Power Stages

A schematic representation of the designed four-way combined power stage is illustrated in Figure 5.1. In order to prevent odd-mode instabilities, the R_{odd} resistors with a value of $10\,\Omega$ are placed midway between adjacent power cells [16]. The collector bias lines have been placed at both sides of the chip to ensure symmetry. The configuration of the bias networks is similar to that used in the matched power cells, with the same bypass capacitors $C_1 = 500$ fF and the series R_2-C_2 for low frequency stability improvement.

5.1.1 Four-Way Input Divider

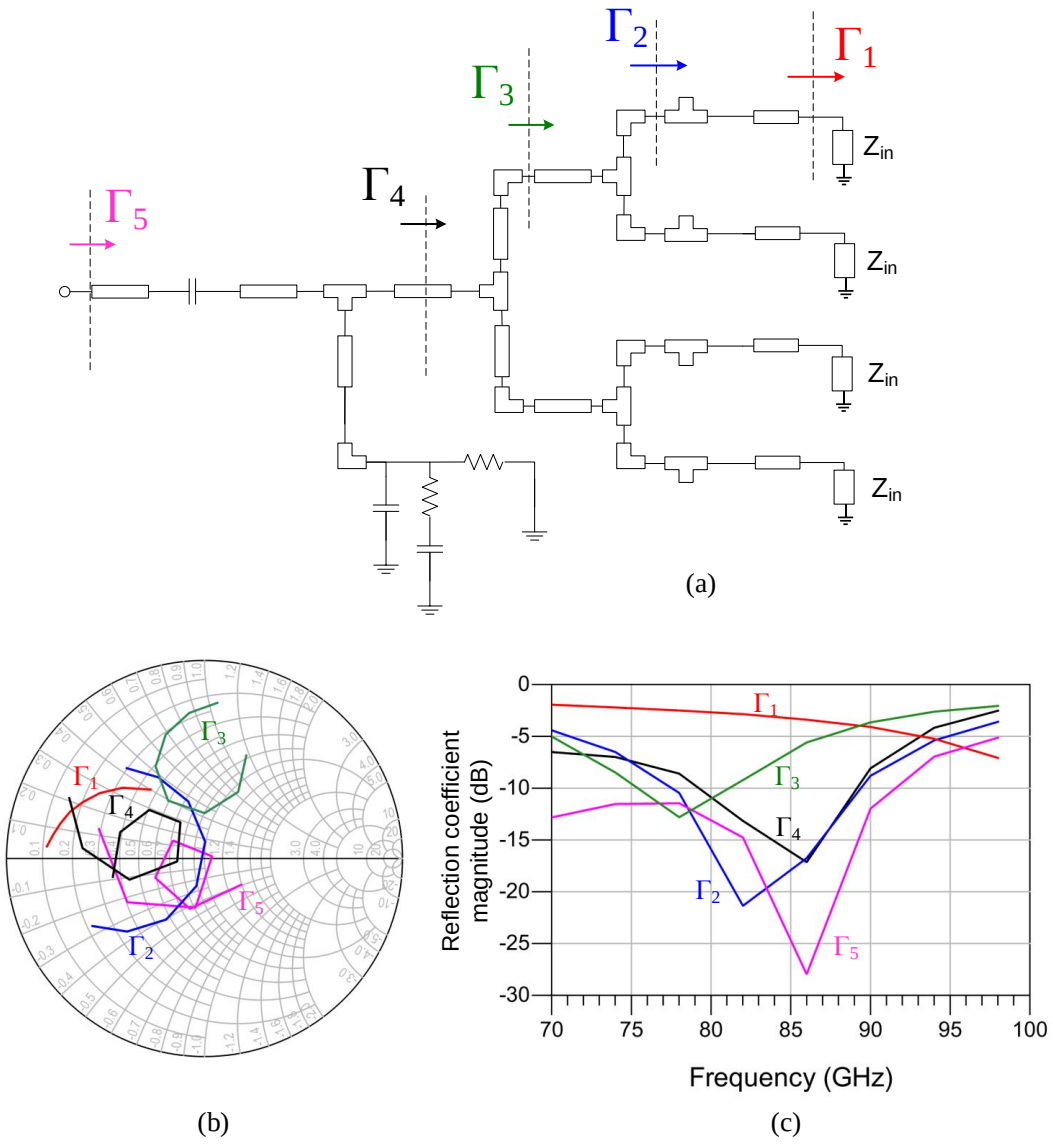


Figure 5.2: Input power divider structure and highlighted design steps (a); corresponding simulated reflection coefficients (b and c).

The input matching/divider structure is designed exploiting the library components based on the 50-Ω CPWs lines and passive structures introduced in Chapter 2. The design is carried out starting from the calculated input impedances of the previously described power cells and moving backward to the 50-Ω input pad of the chip and taking into account also the base bias network. The final optimization goal is a perfect matching condition from the input of the structure. For a target frequency of 86 GHz, the design steps are reported in Figure 5.2, where the matching conditions at every stage are reported also on the Smith chart in the range of frequencies from 70 GHz to 98 GHz.

Based on simulation results, at the designated center frequency of 86 GHz, the losses associated to the input matching network for this power amplifier topology are ≈ 1.5 dB.

5.1.2 Four-Way Output Combiner

A similar approach is used for the design of the output combiner. The starting point in this case is the complex conjugate of the optimum load impedance $Z_{\mathrm{L,opt}}$ of the power cells and the design

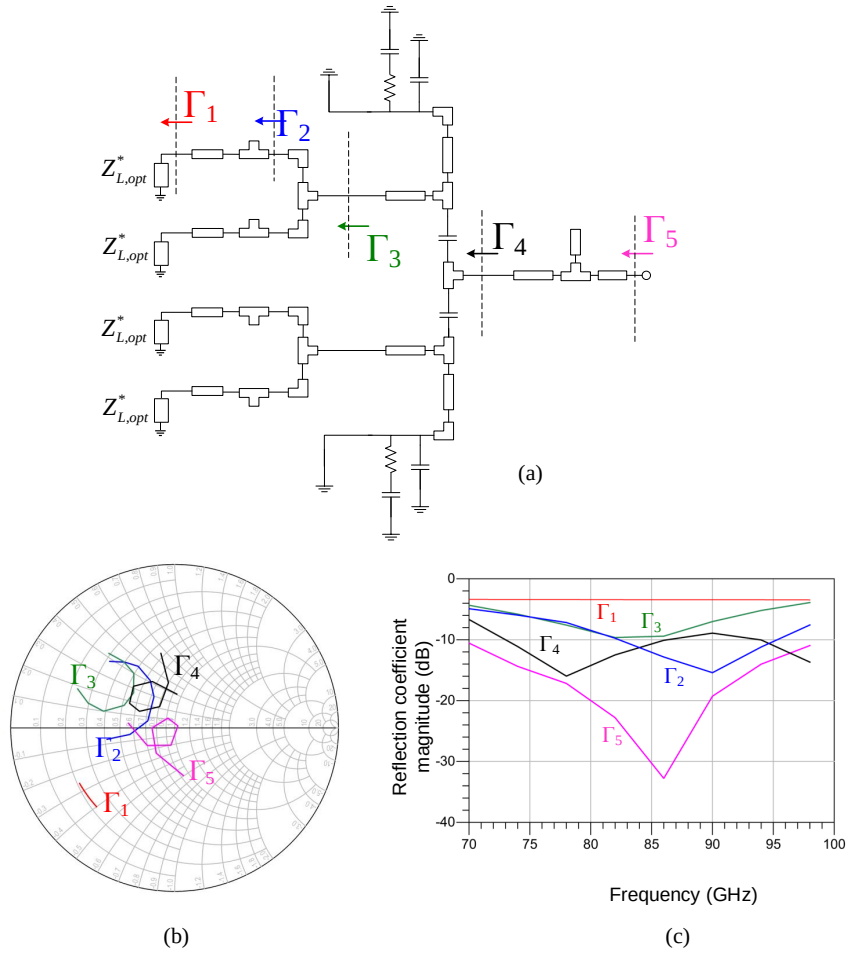


Figure 5.3: Output power combiner design steps (a) and respective simulated reflection coefficients (b and c).

proceeds towards the output pad of the chip as shown in Figure 5.3.

The losses associated to the output combiner network are predicted by simulations around ≈ 1.4 dB. For instance, if each power cell is set to provide 10 dBm of output power, only 14.6 dBm is delivered at the output. A figure of merit which takes into account these losses can be defined as the ratio between the output power and the total input power [15]:

$$\eta_{comb} = \frac{P_{out,comb}}{P_{in,comb}}. \tag{5.1}$$

For the present output combiner, $\eta_{comb} \approx 0.72$ and represents a moderate amount of losses, for which the most significant contributions come from the tee-junctions and the series capacitances, as has been outlined in chapter 2.

5.1.3 Two-Stacked Power Cells

The above described circuit topology has been first investigated employing two-stacked transistors. In Figure 5.4, the MMIC microphotograph of a four-way combined power stage with two-stacked power cells is shown. The bias voltages V_{CC1} and V_{CC2} are set to 4.5 V, resulting in a total collector current of $I_{\mathrm{CC1}} + I_{\mathrm{CC2}} \approx 300$ mA. The chip size is $2.4 \times 1.5\,\mathrm{mm}^2$.

Simulated and measured S-parameters are reported in Figure 5.5. The original design in SAND process is matched at 86 GHz and exhibits a simulated peak $|S_{21}|$ of 8.7 dB at the same frequency. The measured $|S_{21}|$ on a SHARC wafer has a peak of 6.1 dB at 66 GHz and decays at higher frequencies. A quite wideband response has been obtained from 62 GHz to 98 GHz where the return loss is better then 10 dB.

Large-signal simulations and measurements are reported in Figure 5.6. The limited capabilities of the available measurement setup did not allow to evaluate the performance of the power amplifier in gain compression. The best measured performances are obtained at 75 GHz with a maximum measured output power of 17.6 dBm and a small-signal gain of 6.2 dB. The small difference in the small-signal gain with respect to S-parameter measurements can be due to the accuracy of the custom large-signal measurement setup. The maximum measured PAE is around 2.7 % at 75 GHz. The saturated output power predicted by simulation results on the SAND process would have been around 22.6 dBm at 86 GHz. At this frequency, the peak PAE would have been higher than 5 %.

Despite the lower performances obtained from measured results on a SHARC wafer, a good agreement with back-simulations can be observed. Once again, this demonstrates the good modeling and design approach of the circuit.

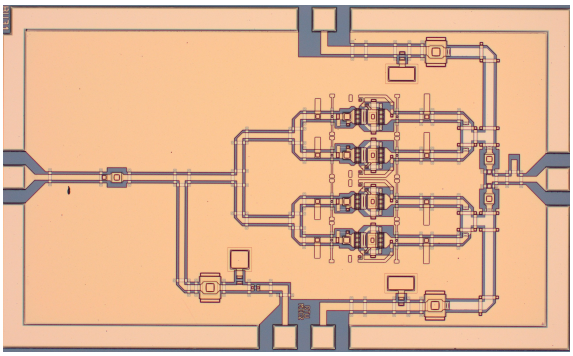


Figure 5.4: Chip microphotograph of the four-way two-stacked power stage. The size is $2.4 \times 1.5\,\mathrm{mm}^2$.

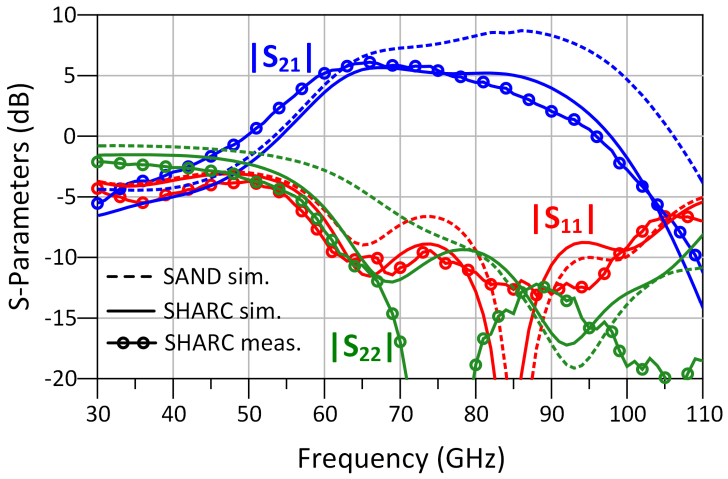


Figure 5.5: Simulated and measured S-parameters of the four-way two-stacked power stage.

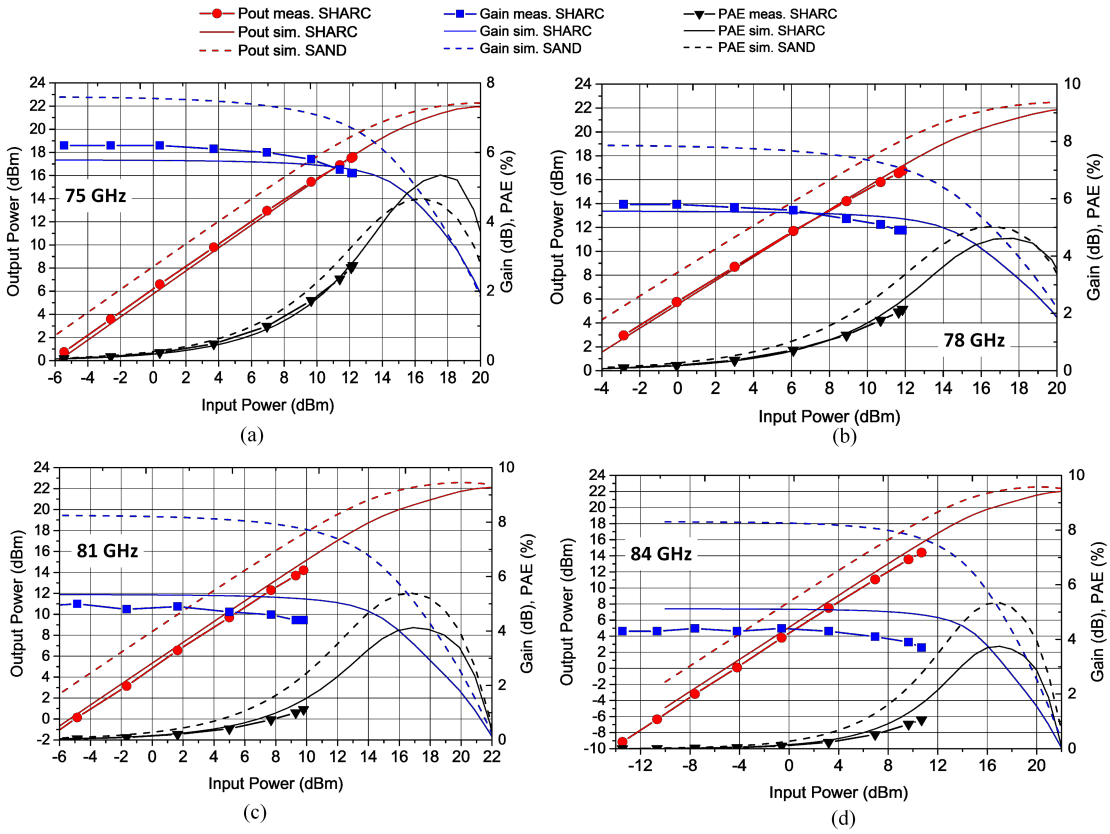


Figure 5.6: Simulated and measured large-signal performances of the four-way two-stacked power stage.

5.1.4 Three-Stacked Power Cells

The same architecture of the previous MMIC power amplifier is adopted with three-stacked power cells. The bias voltage V_{CC} has been raised to 6.5 V and a total collector current of 260 mA resulted. The chip microphotograph of the MMIC, whose size is 2.4×1.5 mm^2, is shown in Figure 5.7. The measured and simulated S-parameters are reported in Figure 5.8. In SHARC implementation, the measured peak $|S_{21}|$ is 7.8 dB at 83 GHz, 1 dB lower than the simulated one. The return loss is better than 10 dB from 67 to 97 GHz. The original design on SAND process is centered at 86 GHz and the simulated peak $|S_{21}|$ is 11.1 dB at 88 GHz.

Large-signal measurements are shown in Figure 5.9 at different frequencies. The highest measured linear gain is 8.8 dB at 81 GHz. At 84 GHz, with 11 dBm of input power, the output power is 18 dBm, showing little indication of gain compression, thus the saturated output power is expected to be higher. Simulation results show an output power at the 1-dB compression point of $P_{\mathrm{out,1dB}} \approx 21$ dBm and a saturated output power of $P_{\mathrm{sat}} \approx 22$ dBm.

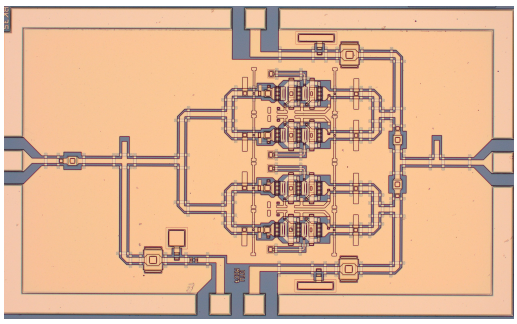


Figure 5.7: Chip microphotograph of the four-way three-stacked power stage. The size is $2.4 \times 1.5\,\mathrm{mm}^2$.

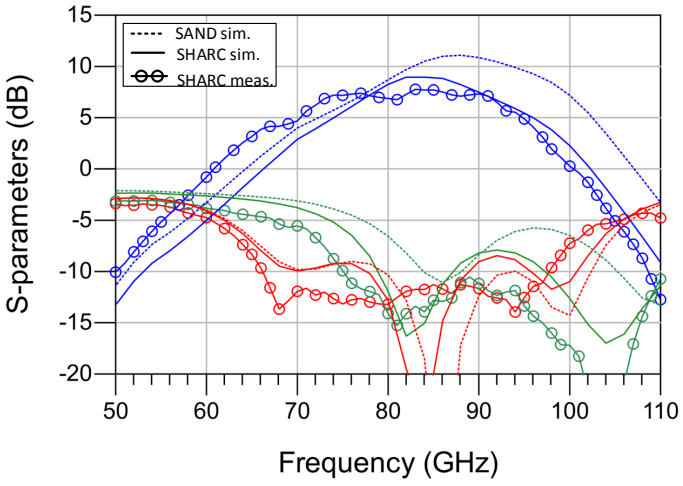


Figure 5.8: Simulated and measured S-parameters of the four-way three-stacked power stage.

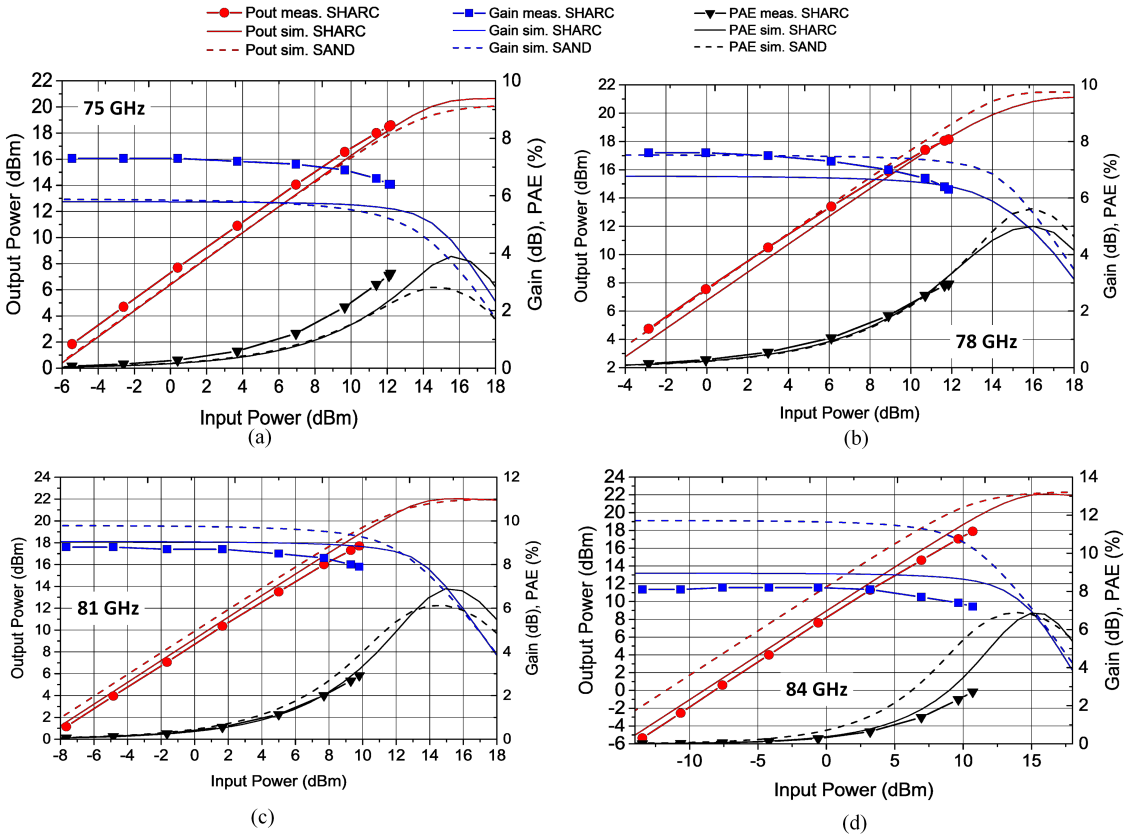


Figure 5.9: Simulated and measured large-signal response of the four-way three-stacked power stage.

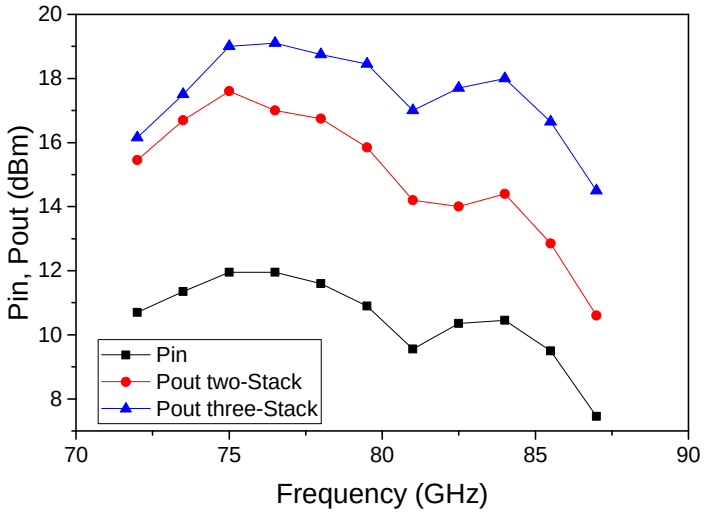


Figure 5.10: Comparison of the measured large-signal broadband frequency response of the four-way two- and three-stacked power stages.

Even though not fully compressed, it is useful to compare the broadband response in large-signal regime of the two four-way power stages presented so far. In Figure 5.10, the meausured output power of the two MMICs are reported as functions of frequency in response of the maximum available input power, also reported in the figure. This confirms in some way the better performances of the three-stacked transistors even when parallel-combined.

5.2 Two-Stage Four-Way Power Amplifiers

In order to obtain higher levels of gain, the presented four-way power stages have been provided with a driver stage in the way shown in Figure 5.11. The design criteria in this case are based on the assumption that the driver should be able to provide enough power to bring into compression the four-way power stage. From the large signal characterizations shown in Figures 5.6 and 5.9, it can be seen that the input 1-dB compression point is approximately 14 dBm and 12 dBm for the two-stacked and three-stacked configurations, respectively. These levels of power should be delivered by the driver stage while operating as linearly as possible [13]. Considering the results on the power cells reported in Chapter 2 and the losses of the interstage matching, some sort of power combination is necessary for the driver to ensure an adequate input power for the second stage.

The interstage matching network has been designed following the principle shown in Figure 5.12: Cutting the circuit at a point between the two stages, it is possible to evaluate the reflection coefficients $\Gamma_{in,2}$ and $\Gamma_{out,1}$. Assuming that the power cells are terminated with the optimum load impedance $Z_{\mathrm{L,opt}}$, the condition $\Gamma_{in,2} = \Gamma^*_{out,1}$ must be satisfied for maximum power transfer. According to the Bode-Fano limitation [78], this condition can be satisfied only in a finite number of frequency points and, as shown in the Smith chart of Figure 5.12, a good matching has been achieved at the design frequency of 86 GHz.

A possible issue related to multiple-stage amplifiers is the stability. Once again, besides

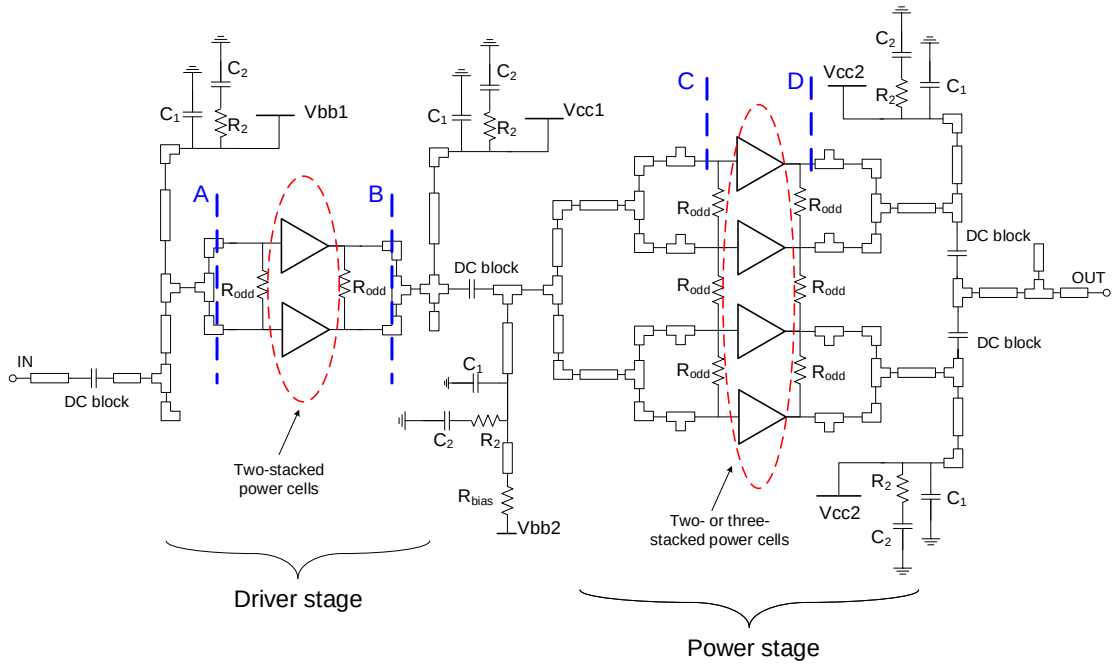


Figure 5.11: Schematic representation of a two-stage four-way combined power amplifier.

input-output stability analysis based on S-parameters, several simulation tests based on pole-zero identification have been conducted to tackle eventual undesired oscillation taking place between the two amplifier stages.

The performance of the power amplifier can be better understood by evaluating the power budget [15], i.e. the contribution of each stage and taking into account the losses in the matching networks. This has been done during the simulation process by probing the RF power at planes A, B, C and D in Figure 5.11. More details on the power budget analysis are given for the following specific cases of two-stage amplifiers featuring two- and three-stacked power cells in the output stage.

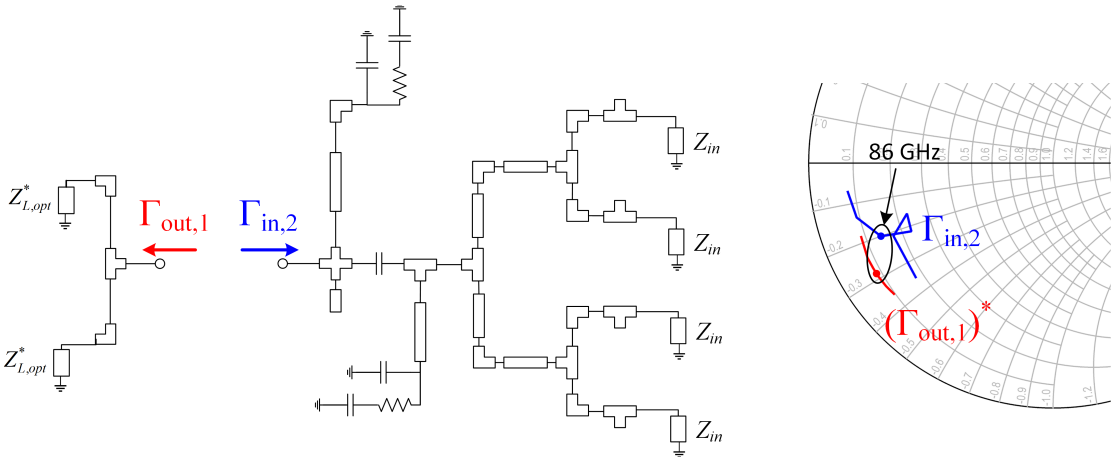


Figure 5.12: Design of the interstage matching network.

5.2.1 Two-Stacked Power Cells

The chip microphotograph of a fabricated two-stage four-way combined power amplifier with two-stacked transistors power cells is reported in Figure 5.13 (size: $2.4 \times 1.5\,\mu\text{m}^2$). Simulated and measured S-parameters are reported in Figure 5.14. The measured S-parameters result quite downshifted in frequency with respect back-simulations. We had already encountered this issue when dealing with the matched power cells, and in particular the three-stacked transistor (Figure 4.4). Indeed, the common feature of these two circuits is the structure of the input matching network employing several bending structures which might present underestimated parasitic capacitances responsible of the downshift. Moreover, the input matching network is accommodated in a quite small area due to the restrictions on the chip size and a good matching could be achieved only in a narrow bandwidth. The measured peak $|S_{21}|$ is 11.4 dB on the SHARC wafer and occurs at 78 GHz. The measured 3-dB bandwidth spans from 69 GHz to 83 GHz while the return loss is better than 10 dB from 76.5 GHz to 82 GHz. The original circuit simulations with SAND models show a peak $|S_{21}|$ of 19.8 dB at 86 GHz, while the matching is centered at 84 GHz with a return loss better than

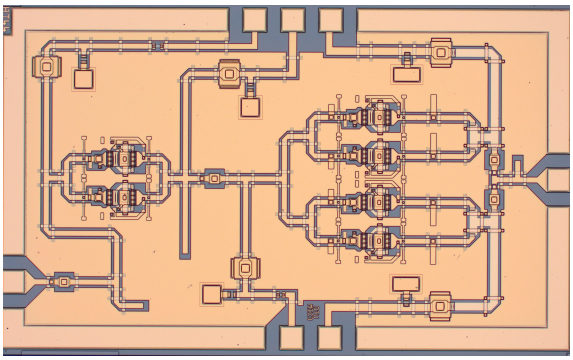


Figure 5.13: Chip microphotograph of the two-stage four-way two-stacked power amplifier.

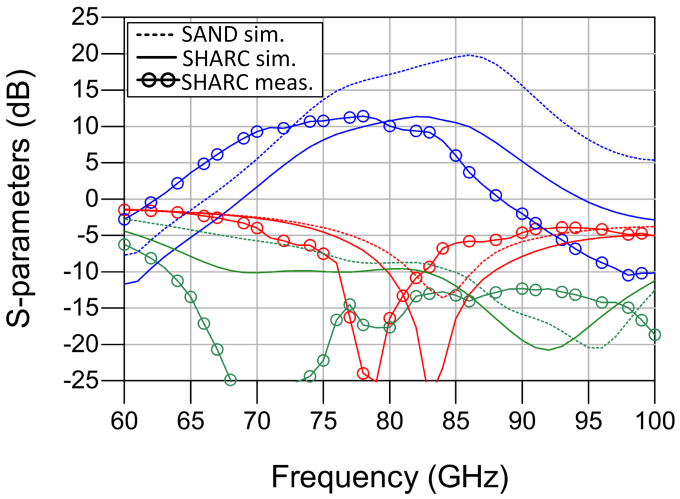


Figure 5.14: Simulated and measured S-parameters of the two-stage four-way two-stacked power amplifier.

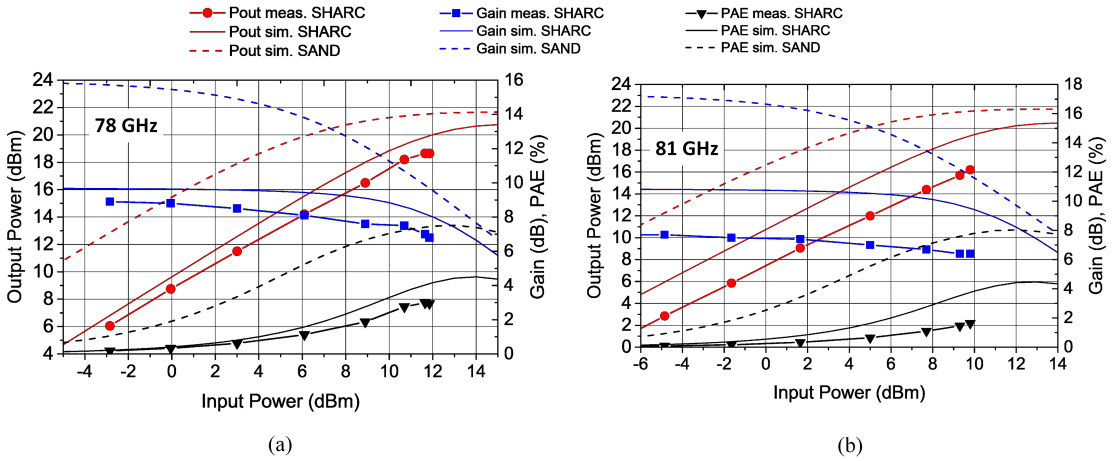


Figure 5.15: Simulated and measured power sweep for the two-stage four-way two-stacked power amplifier at 78 GHz (a) and 81 GHz (b).

13 dB.

In measuring the large-signal performances of this amplifier, a small gain degradation has been observed, probably due to some device deterioration after on/off switching. In Figure 5.15, the simulated and measured power sweeps at 78 GHz and 81 GHz are reported. The maximum level of gain at 78 GHz is 8.9 dB, excessively lower than what S-parameter measurements revealed, and other sites on the wafer of the same circuit did not perform better than this. Even though not in compression, the maximum level of the measured output power is 18.7 dBm and 16.2 dBm at 78 and 81 GHz, respectively. The measured PAE reaches 3 % at 78 GHz. In SAND process, a simulated gain of 17.3 dB, a saturated output power of 21.7 dBm and a peak PAE of 8 % are observed at 81 GHz.

A better insight on the performance of the power amplifier can be obtained by inspecting the simulated power budget at 86 GHz on SAND process. Referring to the schematic of Figure 5.11, the analysis is summarized in Table 5.1: The input matching network exhibits a loss of 2.2 dB. Additional 1.8 dB and 1.4 dB are lost in the interstage matching and output combiner, respectively. The driver and output amplifier stages provide 8.7 dB and 8.5 dB of gain, respectively.

Table 5.1: Simulated power budget analysis at 86 GHz of the two-stage four-way two-stacked power amplifier in SAND process. All quantities are in dBm.

P_{in}	P_A	P_B	P_C	P_D	P_{out}
10	7.8	16.5	14.7	23.2	21.8

5.2.2 Three-Stacked Power Cells

The two-stage power amplifier architecture of Figure 5.11 has been investigated with the output power stage made of three-stacked transistors power cells as well. The bias voltages are set to $V_{cc1} = 4$ V for the driver and $V_{cc2} = 6.5$ V for the power stage. The corresponding total currents are $I_{cc1} = 160$ mA and $I_{cc2} = 2 \times 140$ mA, respectively, which include also the currents flowing through the resistive feedback networks of the power cells. The implemented MMIC power amplifier is shown in Figure 5.16, whose size is $2.4 \times 1.5\,\text{mm}^2$.

The results of S-parameters simulations and measurements are reported in Figure 5.17. The meausred peak $|S_{21}|$ is 13.6 dB and occurs at 77 GHz on the SHARC wafer. The 3-dB bandwidth spans from 74 GHz to 86 GHz while the return loss is better than 10 dB from 76.5 GHz to 82 GHz. As with the previous implementation, the response is downshifted in frequency. The back-simulated peak $|S_{21}|$ occurs at 86 GHz and is about 15 dB, while simulations with SAND models exhibit a peak $|S_{21}|$ of 22 dB. The slightly narrowband response can be attributed mostly to the driver stage whose architecture is similar to the previous amplifier. The same issue concerns the interstage matching network, which could be optimized only for a limited frequency range.

The best performances under large-signal regime are obtained at 78 GHz (Figure 5.18(a)),

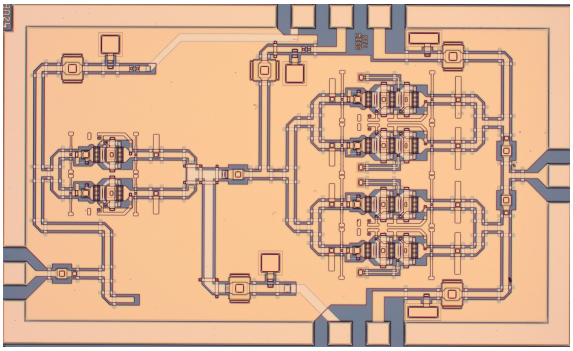


Figure 5.16: Chip microphotograph of the two-stage four-way three-stacked power amplifier.

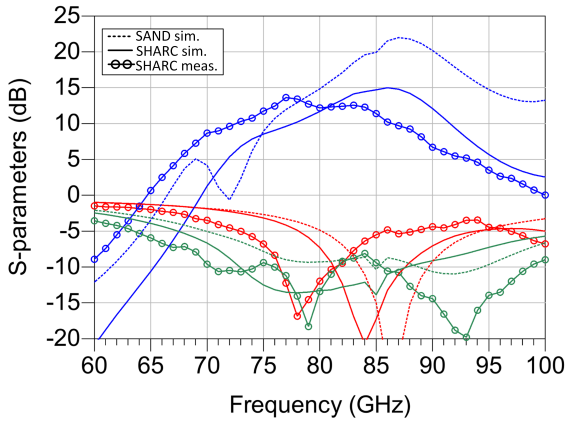


Figure 5.17: Simulated and measured S-parameters of the two-stage four-way three-stacked power amplifier.

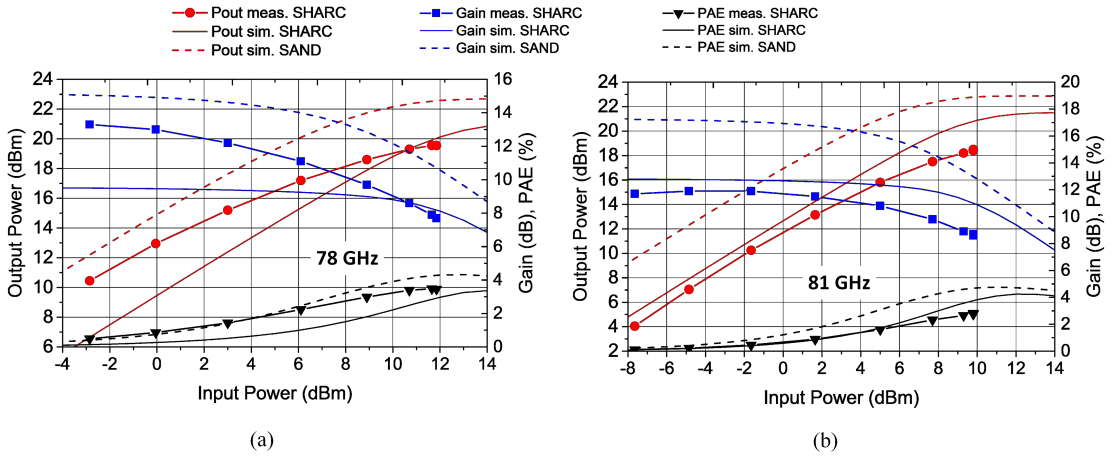


Figure 5.18: Simulated and measured power sweep for the two-stage four-way three-stacked power amplifier at 78 GHz (a) and 81 GHz (b).

where the measured saturated output power is around 19.6 dBm and the peak PAE is 3.5 %. However back-simulations and measurement results on the SHARC wafer come close to each other at 81 GHz (Figure 5.18(b)), as already predicted by S-parameters characterization. At 81 GHz, the simulated gain on SAND models is 12.8 dB, against 8.7 dB of the measured one of the SHARC wafer. The simulated saturated output power and peak PAE on SAND are 21.6 dBm and 4.8 %, respectively.

Table5.2 summarizes the simulated power budget at 86 GHz on SAND process. The input matching network exhibits a loss of 2.3 dB. Additional 1.7 dB and 1.6 dB are lost in the interstage matching and output combiner, respectively. The driver and output amplifier stages provide 10 dB and 8.2 dB of gain, respectively.

Table 5.2: Simulated power budget analysis at 86 GHz of the two-stage four-way three-stacked power amplifier in SAND process. All quantities are in dBm.

P_{in}	P_A	P_B	P_C	P_D	P_{out}
10	7.7	17.7	16	24.2	22.6

The measured results of the two-stage amplifiers with two- and three-stacked transistors can be better compared by plotting their broadband frequency response under large-signal operation. In Figure 5.19, the maximum available input power and the maximum measured output power from the two amplifiers are reported as functions of frequency. Apart from the 72 GHz point where the amplifier with two-stacked transistors exhibits a slightly higher output power, this plot confirms the overall best performances of the three-stacked power cell even in a two-stage configuration. A noticeable characteristic observed in Figure 5.19 is that the three stacked power cell is clearly operating in gain compression as its output power remains almost constant and barely follows the input power profile, in contrast with the two-stacked power cell which operates more linearly with the same input power.

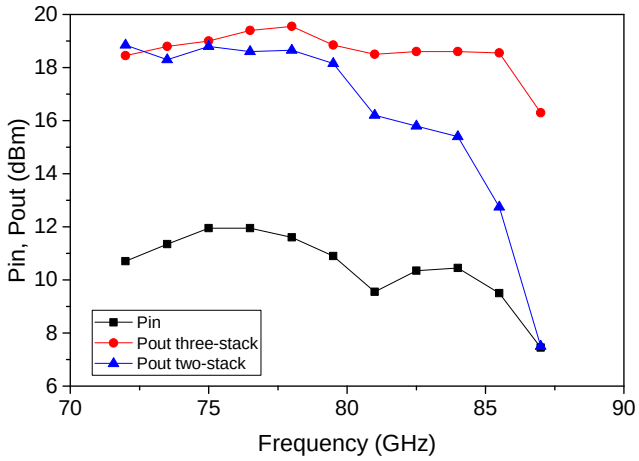


Figure 5.19: Comparison of the measured large-signal broadband frequency response of the two-stage four-way two- and three-stacked power amplifiers.

5.3 Eight-Way Combined Power Amplifiers

An attempt to further increase the output power is pursued by parallel combining up to eight power cells. Two-stacked transistors have been combined as shown in the architecture of Figure 5.20. Successively, this power stage has been provided with a four-way parallel combined driver stage. The design of the power dividers/combiners and interstage matching networks followed the same procedure shown previously for the four-way power amplifiers. The performances of the single stage and two-stage eight-way power amplifiers are reported in the following.

5.3.1 Two-Stacked Power-Stage

Actually, the eight-way combined power stage is designed for operation at 94 GHz. The circuit schematic and the chip microphotograph are reported in Figures 5.20 and 5.21. The chip size is 2.4×3 mm2. Given the high number of power cells, a considerable amount of dc power is required. With the collector bias voltage $V_{\mathrm{CC}} = 4.5$ V and and the total collector current approaching 0.6 A, the absorbed dc power is around 2.7 W. Considerable losses occur in the power divider and combiner: Simulation results at 94 GHz revealed a loss of 2.4 dB in the former and 2.7 dB in the latter, representing an impact of more than 5 dB on the overall gain performances.

S-parameters simulations and measurements of the eight-way power stage are reported in Figure 5.22. Apart from the peak value of 4.3 dB at 54 GHz, the highest measured level of $|S_{21}|$ in the band of interest occur at 80 GHz and is 3.2 dB on the SHARC wafer. The measured return loss is better than 10 dB from 76 GHz to 96 GHz. The original design on SAND models, on the other hand, exhibits a peak $|S_{21}|$ of 7.1 dB at 92 GHz and a return loss better than 10 dB from 80 GHz to 98 GHz.

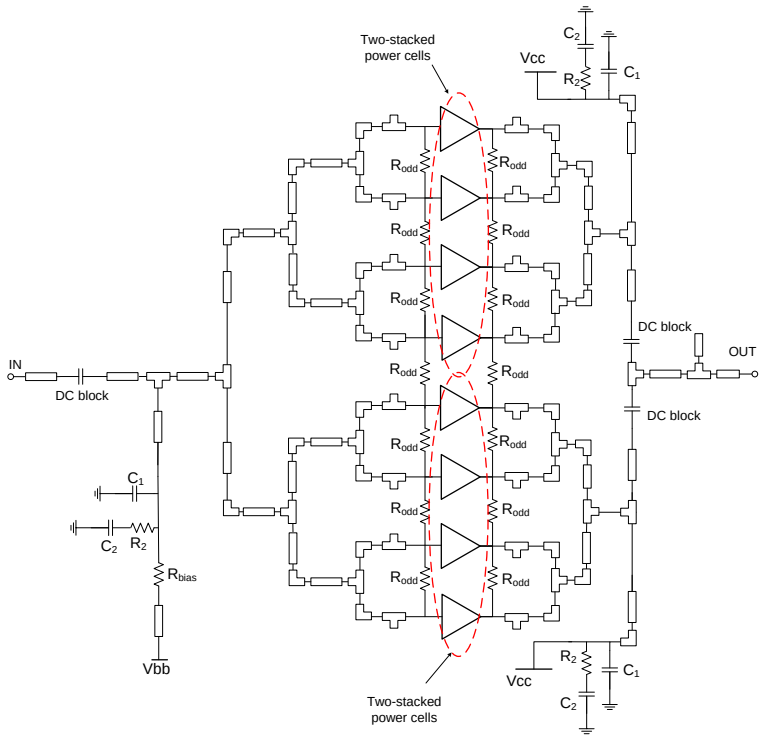


Figure 5.20: Circuit schematic of the eight-way two-stacked power stage.

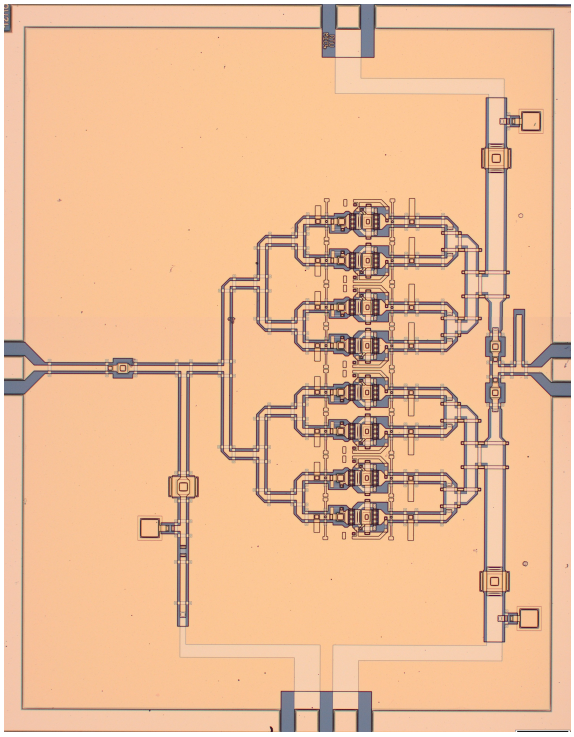


Figure 5.21: Chip microphotograph (b) of the eight-way two-stacked power stage. The chip size is 2.4×3 mm^2.

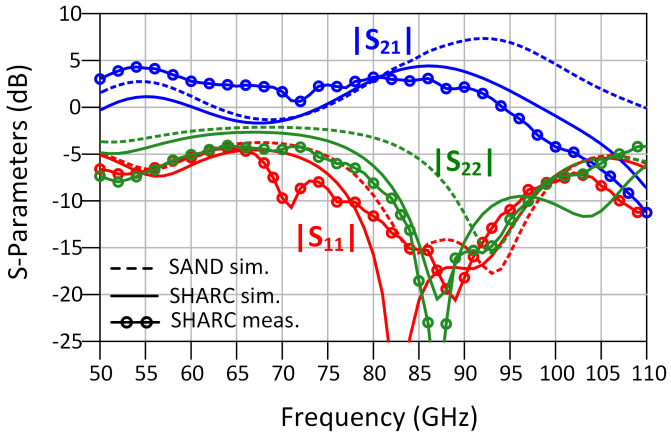


Figure 5.22: Simulated and measured S-parameters of the eight-way two-stacked power stage.

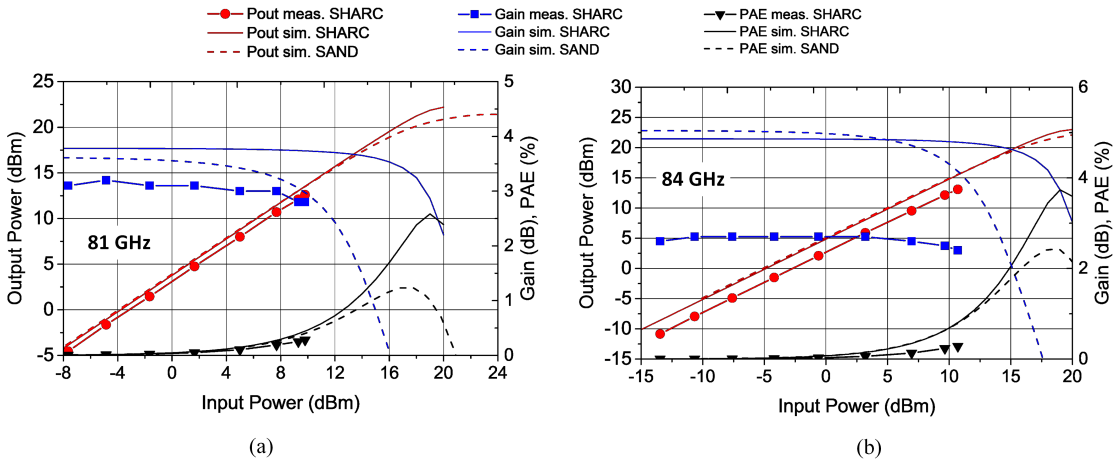


Figure 5.23: Simulated and measured large signal response of the eight-way two-stacked power stage.

Large-signal characterization results are reported in Figure 5.3.1 at 81 GHz and 84 GHz. In both cases, very small compression can be achieved and the maximum measured output power is 13.1 dBm with an input power of 10.7 dBm at 84 GHz. The projected saturated output power predicted by original simulations with SAND models is 22.6 dBm at 84 GHz. However, at the target frequency of 94 GHz, the simulated saturated output power reaches 25 dBm.

5.3.2 Two-Stage Two-Stacked Power Amplifier

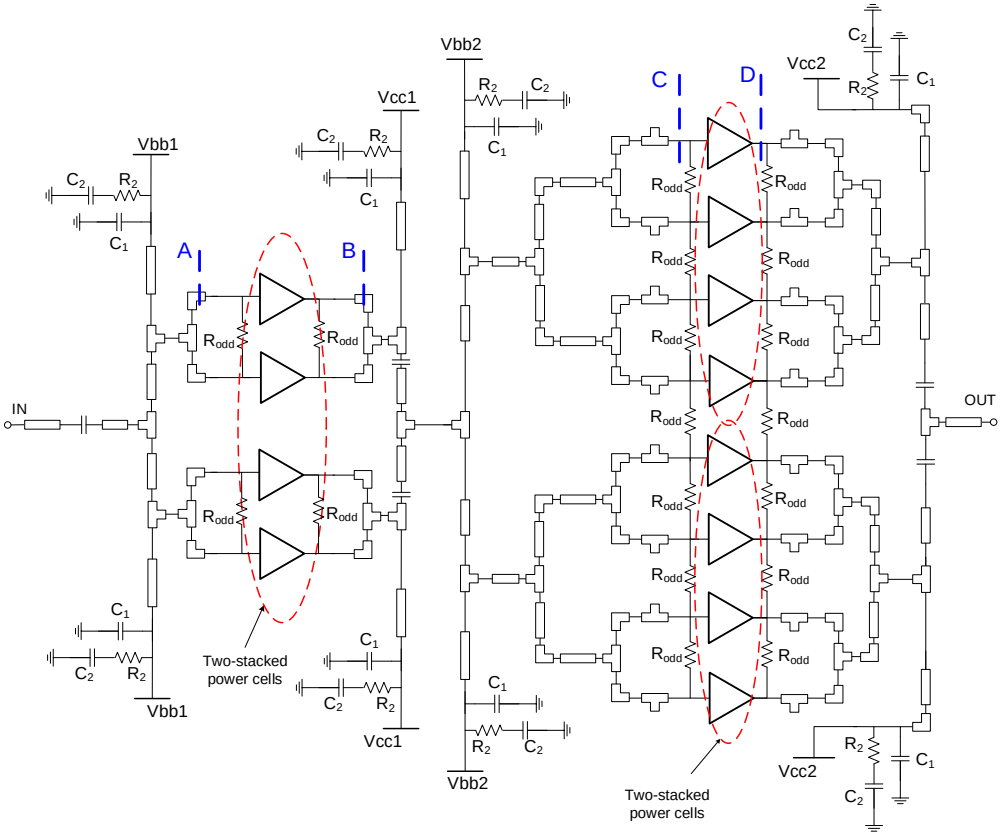
The schematic representation of a two-stage amplifier employing the eight-way power stage presented in the previous section is illustrated in Figure 5.24(a). The driver-stage is a four-way combined amplifier composed of two-stacked transistors. The chip microphotograph is shown in Figure 5.24(b) and the size is $2.4 \times 3\,\text{mm}^2$. The S-parameters measurements of this power amplifier in SHARC process are reported in Figure 5.25. The measured input return loss results quite downshifted in frequency and exhibits sharper minima with respect to back-simulations performed on the same process. The maximum measured gain is downshifted as well and reaches 11 dB at 74 GHz. Back-simulations, on the other hand, result in a peak $|S_{21}|$ of 10.1 dB at 86 GHz and a 3-dB bandwidth from 74 GHz to 93 GHz. Given the considerable complexity of the design, the complete modeling of the power amplifier revealed more difficult and prone to inaccuracies, so a moderate discrepancy between measurements and back-simulations are observed, especially at higher frequencies. The simulated S-parameters of the original design on SAND transistor models are centered at 86 GHz. In this case, the peak $|S_{21}|$ occurs at 89 GHz and is 17.4 dB. The 3-dB bandwidth ranges from 77 GHz to 94 GHz.

Large-signal simulations and measurements are compared at 78 GHz and reported in Figure 5.26. The measured gain at low input power is 9.9 dB at this frequency, which seems a little optimistic with respect to S-parameters measurements probably due to uncertainties on the calibration of the large-signal test setup. The measured maximum output power is 20.2 dBm, which is by no means the saturated one and quite higher output power can be expected if the amplifier were driven into deeper compression by a higher input. Slightly better performances are achieved at 75 GHz, where a small-signal gain of 12.6 dB and a maximum output power of 21.4 dBm were registered experimentally. Large-signal simulations on SAND and SHARC processes show approximately the same saturated output power of 24 dBm, but they differ in the higher small-signal gain for the SAND process.

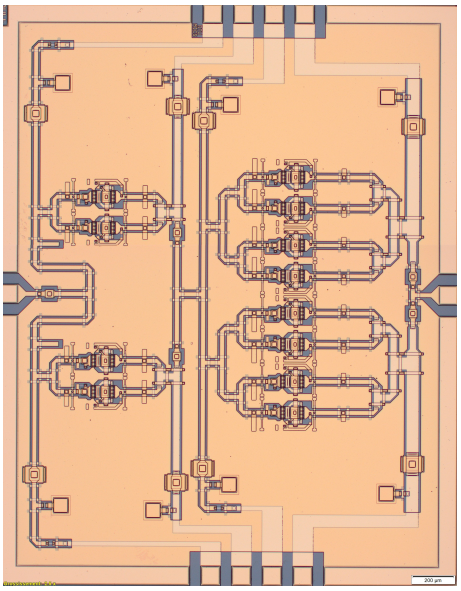
For this power amplifier, a power budget analysis at the target frequency of 86 GHz and with SAND transistor models has been carried out as well to get a better understanding of the contribution of each stage to the overall performance. Referring to the selected planes A, B, C and D in Figure 5.24(a), Table5.3 summarizes the corresponding power levels. With an input power of 10 dBm, the amplifier is not fully compressed and the amplifier stages provide a substantial gain. For instance, the driver stage provides around 10.6 dB of gain while the output power stage provides 9.5 dB. The highest losses occur in the interstage matching network, which exhibits an attenuation of 2.2 dB, while 1.6 dB and 1.7 dB are lost in the input and output matching networks.

Table 5.3: Simulated power budget analysis at 86 GHz of the two-stage eight-way two-stacked power amplifier in SAND process. All quantities are in dBm.

P_{in}	P_A	P_B	P_C	P_D	P_{out}
10	8.4	19	16.8	26.3	24.6



(a)



(b)

Figure 5.24: Schematic (a) and chip microphotograph (b) of the eight-way two stage power amplifier. The chip size is 2.4×3 mm^2.

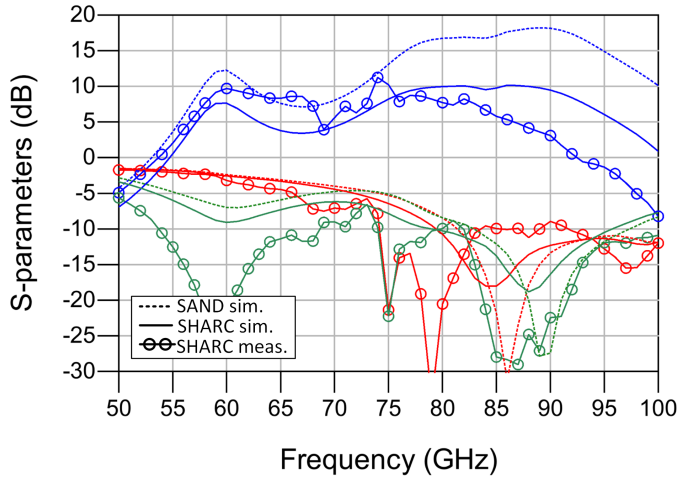


Figure 5.25: Simulated and measured S-parameters of the eight-way two stage power amplifier.

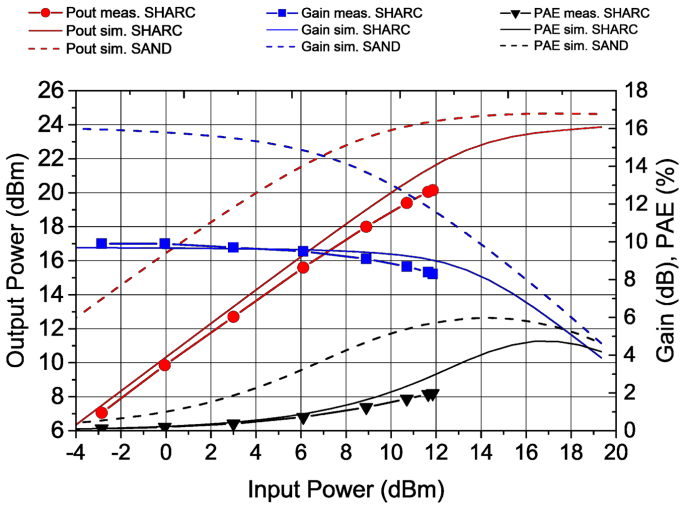


Figure 5.26: Simulated and measured power sweep for the eight-way two stage power amplifier at 78 GHz.

5.4 Summary

In this chapter, the implementation and measurement results of full MMIC power amplifiers based on the previously described stacked-transistor power cells have been reported. The power cells building blocks have been combined in parallel by means of four-way and eight-way CPW-based corporate topologies. The parallel combined power stages have been tested in stand alone configurations and then integrated with a driver stage for increasing the gain performances. Also in this case, all the designs were optimized based on SAND models and realized on a SHARC wafer.

A four-way two-stacked power stage exhibits a measured peak small-signal gain of 6.1 dB at 66 GHz, falling below 5 dB at frequencies higher than 80 GHz. Simulations on the SAND model, instead, show 8.7 dB at 86 GHz. The saturated output power could only be estimated by simulations as the measurement setup did not allow to bring the power amplifier into compression. 22.6 dBm at 86 GHz would have been achieved on a SAND wafer, while the highest measured output power on the SHARC one is 17.6 dBm at 75 GHz. A similar circuit architecture with three-stacked transistors exhibits a measured small-signal gain of 7.8 dB at 83 GHz and a maximum measured output power of 18 dBm at 84 GHz. These results confirm once again the better performances of the three-stacked transistor over the two-stacked one. If paired with an integrated driver stage formed by two-way combined two-stacked transistors, the gain can be increased up to 13.6 dB at 77 GHz and the output power can approach saturation: At 78 GHz, 19.6 dBm has been obtained from the three-stacked power stage.

Eight-way combined two-stacked topologies have been finally realized both in a stand alone and with a driver stage. In these cases, the amount of losses occurring in the divider and combiner circuits become important and the performance improvements do not scale as they would in an ideal case. Furthermore, their complexity makes their behavior more difficult to predict in the design process. As a result, some more discrepancy between simulations and measurements are observed. That said, the two-stage eight-way power amplifier exhibit the highest measured output power among the circuits presented so far: 21.4 dBm is registered at 75 GHz and nearly 25 dBm has been estimated in simulations.

In summary, two power combining techniques – the novel series voltage stacking and the more traditional parallel configuration – have been applied concurrently in order to pursue the best possible performances. Even though some limitations exist in both directions, remarkable results have been finally obtained.

CHAPTER 6

Conclusion

The focus of this project has been the investigation of suitable topologies for the implementation of E-band power amplifiers in InP DHBT technology. The stacked-transistor architecture has been analyzed in detail in small- and large-signal regimes, taking into account also layout-related parasitics by means of extensive EM simulations. Guidelines for the design procedure of such a structure are provided as well. Limiting factors related to the particular technology have been especially identified in unavoidable layout parasitic effects. In particular, the finite length of the interconnects between consecutive stages introduce undesirable phase misalignment between the collector voltages, resulting in early compression. However, a lower limit for the spacing between consecutive transistors exists which is dictated by the process design rules. A technology with a higher scale of integration, such as SiGe, would take more benefits from this approach, as has been widely demonstrated in the literature.

Notwithstanding, considering key parameters of power amplifiers, the three-stacked transistor topology demonstrated here on InP DHBT technology seem to exhibit a good trade-off with respect to the two-stacked and four-stacked transistors. The two-stacked one can be advantageous for its small area occupancy and lower bias voltage, but has lower gain and power capabilities. The four-stacked is affected by a too early compression and cannot reach high saturated power. Moreover, its high bias voltage is responsible for a degraded PAE. On the other hand it has a very high small-signal gain. These results have been verified experimentally on fabricated MMIC matched power cells. For instance, at 81 GHz, the saturated output power of the three- and four-stacked transistor power cells are comparable, being 15 dBm and 14.9 dBm, respectively. The peak PAE, however, is higher for the former one, 5.2 % against 3.8 %, because of the lower bias voltage. Small-signal gain performances are better for the four-stacked power cell, exhibiting a peak $|S_{21}|$ of 11.4 dB at 83 GHz against 8.6 dB of the three-stacked one.

Once established the limit of voltage power combining, a higher output power can be achieved by parallel power combining. In this regard, this project dealt with the implementation of full MMIC multiple-way power amplifiers as well. The designed stacked power cells have been extensively employed in four- and eight-way combined power stages. For some of them, driver amplifier stages have allowed to increase the gain. The highest measured output power has been achieved by a two-stage eight-way combined two-stacked configuration which features higher than

21.4 dBm at 75 GHz.

This project is based on a 0.7 μm InP DHBT technology developed at III-V Lab whose main characteristics and figures of merit have been recalled in this thesis. It should be noted that two variations of the same technology are available: one is optimized for high-speed mixed-signal applications and the other for analog power applications. All the designs are based and optimized for the latter, but the fabricated circuits and measured results are from the former. Because of this mishap, the obtained results are slightly below the expectations. Back-simulations, however, were carried out and the design principles could be successfully validated.

Even if slightly below the current state-of-the-art of E-band power amplifiers, this work proposes some new topologies and design approaches which, in the author's knowledge, have not been encountered in InP DHBT technology and could be of inspirations for further developments.

6.1 Future Works

Throughout this work, little attention has been given to efficiency optimization. In order to achieve decent levels of output power, DHBT devices need a considerable amount of dc current to operate in Class A for linear mode. This condition entails a high level of dc power consumption. Thus, further investigations are worth to be carried out in order to improve the efficiency, especially in power back-off. Many techniques are known for efficiency enhancements, but they find wide applications only at microwave or lower mm-wave frequencies. Extending these techniques or introducing new ones at higher mm-waves could be one of the next research directions.

Related to efficiency is loss minimization. As is briefly described in this work, passive structures represent an important part for MMIC design and their modeling is essential for effective design, but loss minimization requires a technological approach: a thicker metal layer and a thicker dielectric could result advantageous for power amplifier implementation. With the same goal of improving performances, other power combining techniques could be investigated as well.

It is true that wireless communications will take place at mm-wave frequency and the E-band represents one of the most suitable ranges. Many research efforts, however, are being exerted with the aim of exploiting even higher frequencies and eventually sub-teraherts ranges in order to increase the transmission capacity. Going on this direction requires aggressive size down-scaling of transistors and eventually different design approaches. The stacked transistor architecture could find increasingly wide application in this context where the maximum sustainable voltages decrease steadily. Moreover, InP devices are still unsurpassed in fact of frequency of operation and are envisioned to stay at the forefront in many high frequency applications. In light of these considerations and objectives, this project paves the way towards further developments in mm-wave power amplifiers design techniques.

APPENDIX **A**

Measurement Setup

S-parameters measurements for all MMIC power amplifiers have been carried out on wafer using RF GSG probe tips and the VNA MS4647 by Anritsu. For large-signal measurements, a custom-made test setup has been implemented, whose conceptual representation is shown in Fig. A.2(a): a low-frequency sinusoidal signal is generated by the frequency synthesizer 68169B by Anritsu; the required E-band signal is then obtained by means of the frequency multiplier ($\times 6$) RPG AFM6 capable of a maximum output power of 7 dBm. A 0-50 dB variable attenuator and the 70-90 GHz medium power amplifier (MPA) RPG 7090 are used together to vary the input power fed into the device under test (DUT). The output power level is measured with the power sensor W8486A and the power meter N1914A by Agilent. A shortcoming with this setup is that the maximum available power at the input probe tip is limited and its frequency dependence over the E-band range is reported in Fig. A.2(b). This did not represent an issue in measuring simple power cells, but revealed as a restriction for multiple power-combined circuits, which could not be operated in saturation.

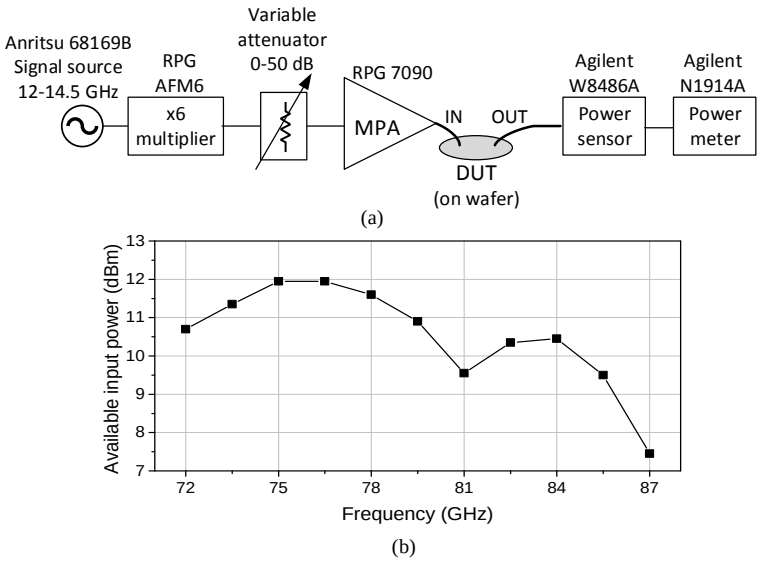
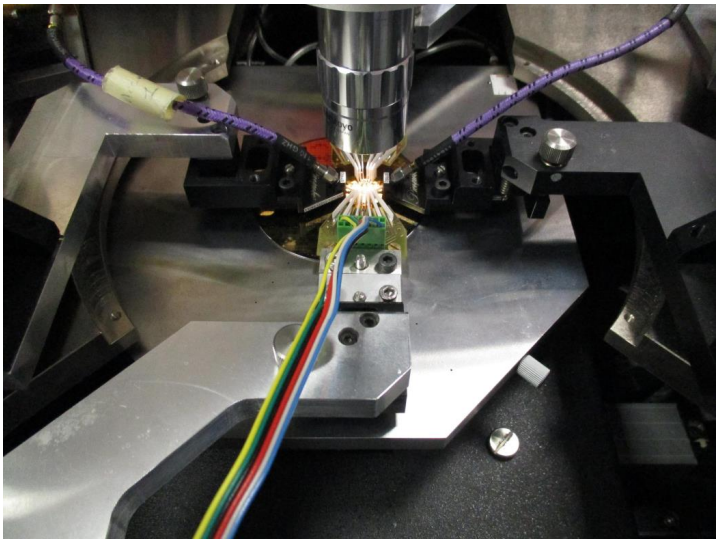


Figure A.1: Conceptual representation of the large-signal measurement setup (a) and calibrated maximum available input power at different frequencies (b).

(a)



(b)

Figure A.2: Measurement equipment (a) and detail of the probe station with on-going on-wafer measurement (b).

APPENDIX **B**

Appended Papers

1. M. Squartecchia, V. Midili, T. K. Johansen, J.-Y. Dupuy, V. Nodjiadjim, M. Riet, and A. Konczykowska, "75 GHz InP DHBT Power Amplifier Based on Two-Stacked Transistors," *Proceedings of the Asia Pacific Microwave Conference (APMC),* 2017.

2. M. Squartecchia, T. K. Johansen, V. Midili, "Design Procedure for Millimeter-wave InP DHBT Stacked Power Amplifiers," *Proceedings of the International Workshop on Integrated Nonlinear Microwave and Millimetrewave Circuits (InMMiC),* 2015.

3. M. Squartecchia, B. Cimoli, V. Midili, T. K. Johansen, V. Zhurbenko, "Design of a Planar Ultra-Wideband Four-Way Power Divider/Combiner Using Defected Ground Structures," *Proceedings of the 48^{th} European Microwave Conference (EuMC),* 2017.

“75 GHz InP DHBT Power Amplifier Based on Two-Stacked Transistors”

75 GHz InP DHBT Power Amplifier Based on Two-Stacked Transistors

Michele Squartecchia [#1], Virginio Midili [#], Tom K. Johansen [#], Jean-Yves Dupuy [*], Virginie Nodjiadjim [*], Muriel Riet [*], Agnieszka Konczykowska [*]

[#] *Department of Electrical Engineering, Technical University of Denmark*
348 Ørsted Plads, 2800 Kongens Lyngby, Denmark
[1]micsqua@elektro.dtu.dk

[*] *III-V Lab (joint lab of Nokia Bell Labs, Thales, and CEA-Leti)*
1 avenue Augustine Fresnel, F-91767, Palaiseau Cedex, France

***Abstract*—In this paper we present the design and measurements of a two-stage 75-GHz InP Double Heterojunction Bipolar Transistor (DHBT) power amplifier (PA). An optimized two-stacked transistor power cell has been designed, which represents the building block in the power stage as well as in the driver stage of the power amplifier. Besides the series voltage addition of the stacked structure, parallel power combining techniques were adopted to increase the output power of the MMIC amplifier, with four-way and eight-way corporate power combiners at the driver and power stages, respectively. At 75 GHz, the power amplifier exhibits a small signal gain of G = 12.6 dB, output power at 1-dB compression of $P_{out,1dB}$ = 18.6 dBm and a saturated output power of P_{sat} > 21.4 dBm.**

Keywords—Indium phosphide; double heterojunction bipolar transistor (DHBT); power amplifier; stacked transistor; power combining.

I. INTRODUCTION

The E-band frequency range is well suited for applications like backhaul wireless communications (71-76 GHz and 81-86 GHz), automotive radars (77 GHz), imaging (94 GHz), and many others. In such systems, power amplifiers design and optimization are of paramount importance for reliable signal transmission. To operate at these frequencies, semiconductor devices have been heavily downscaled for achieving high values of f_T and f_{max} [1]. The downside of this trend is the subsequent reduction of the breakdown voltage and output power. Many efforts have been deployed to overcome this drawback and the most widespread solution is the stacked-transistor topology, consisting of two or more transistors connected in series in a cascode-like configuration [2]-[4]. In this way the overall output voltage swing can be significantly increased as it is shared equally among the transistors. The main difference with respect to the standard cascode is that the base (or gate) terminal of the common-base stage is connected to ground through a finite impedance (typically a capacitance) which plays an important role for interstage matching and makes the base (or gate) voltage oscillate together with the collector (or drain), preventing voltage breakdown. Another beneficial outcome of the stacked topology is an increased optimum load impedance, which results in a smaller transformation ratio of the matching network improving the overall power amplifier efficiency. This is an important aspect to consider also for low loss parallel power combining as a mean to increase the output power [5].

So far, the stacked-transistor topology has been widely investigated on silicon-based devices due to their limited breakdown voltage, especially for CMOS transistors [6]. This work represents an attempt to extend the concept to InP DHBTs. We propose a 75-GHz two-stage InP DHBT MMIC power amplifier using optimized two-stacked transistors as basic power cells. In the power stage, they are combined in parallel by means of an eight-way corporate power combiner implemented with coplanar waveguides (CPW). The same power cells are used in the driver stage in a four-way parallel combined topology. The InP DHBT technology used in this design is briefly described in Section II. In Section III, the main features of the power cell and the full MMIC design are illustrated. In Section IV, measurements results in small and large signal regimes are reported. Conclusions and comments follow in Section V.

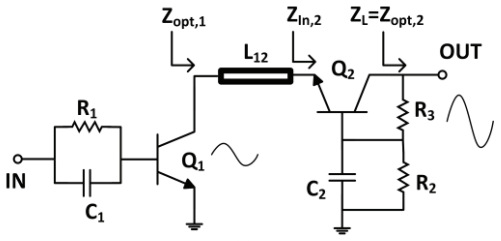
II. INP DHBT TECHNOLOGY

The InP DHBT technology employed in this design is optimized for high speed mixed-signal ICs and has been developed at III-V Lab [7]. Four-finger transistors featuring total active area of 4×0.7×10 μm^2, breakdown voltage BV_{ceo}=4.75 V and f_T/f_{max}=340/370 GHz are used in the power cells. A modified UCSD HBT model extracted from previous measurements is used in simulations to predict their behavior [8]. Passive devices and interconnects are realized on a three-layer stack process (met1-met3). It comprises 40Ω/□ NiCr resistors and 0.49 fF/μm^2 Si_3N_4 MIM capacitors. Power combining, matching networks and bias lines are realized in CPW using PtTiAu metallization.

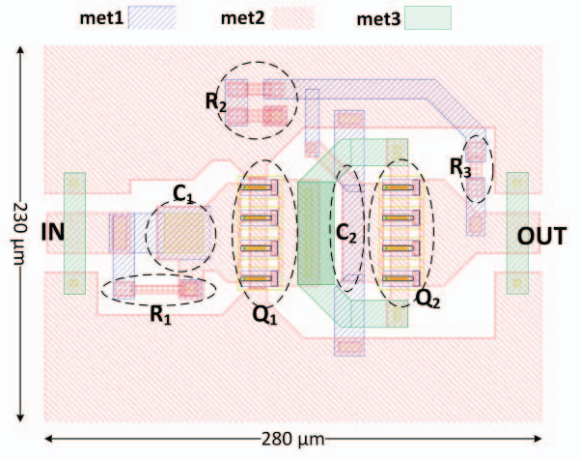
III. CIRCUIT DESIGN

A. Power cell

The schematic of the two-stacked transistor power cell is shown in Fig. 1a, where Q_1 and Q_2 represent the four-finger DHBT devices. At the base input of the common-emitter stage, the parallel R_1-C_1 is inserted for stabilizing the power cell at low frequencies. Besides stabilization, R_1 is also part of the base bias network (omitted in the Figure). The two transistors



(a)



(b)

Fig. 1. Two-stacked transistor power cell: (a) schematic view and (b) layout view (bias network omitted).

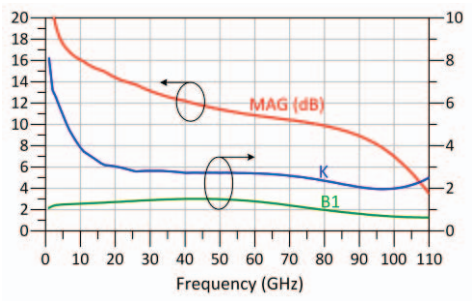
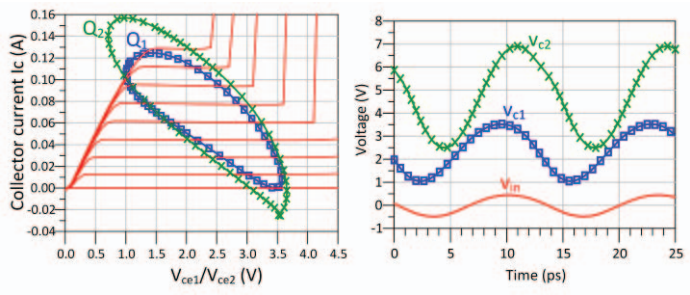


Fig. 2. Simulated Maximum Available Gain (MAG), stability factor K and stability meausre $B1$ of the two-stacked transistor power cell



(a) (b)

Fig. 3. Simulated dynamic load-line (a) and voltage waveforms (b) taken at the collector nodes of Q_1 and Q_2 with saturated output power P_{sat}=18 dBm and Z_L=$Z_{opt,2}$=14+j8 Ω at 75 GHz.

are biased for Class A operation and such that V_{ce1}=V_{ce2}=2.4 V, with a DC collector current of I_c=60 mA. This is accomplished by means of a self-bias resistive voltage divider R_2-R_3. The first step in the design process of the stacked-transistor is a load-pull simulation test for the determination of the optimum load impendance $Z_{opt,1}$ of Q_1. For optimum power transfer, the input impedance of the common-base stage $Z_{in,2}$ should be matched to this value. An approximated analytical formula for calculating $Z_{in,2}$ is given in [9], where its dependence on the base capacitance C_2 and output load Z_L is proved. C_2 and Z_L determine also the magnitude and phase of the RF output voltage, which should satisfy the principal objective of the stacked transistor, that is in-phase voltage addition. A straightforward procedure to find C_2 and Z_L is reported in [10]. Besides self-bias, the role of the feedback network R_2-R_3 is to stabilize the power cell at all frequencies and their values are chosen in such a way that the output power and gain are only negligibly affected. The interconnection of finite length between the two transistors is modeled in the schematic by the transmission line L_{12}, which plays a role also for interstage impedance matching. The layout of the stacked power cell is shown in Fig. 1b, where the single components are highlighted. Their values have been chosen after an iterated optimization process based on EM-circuit co-simulations carried out on ADS Momentum. In Table I, those values are summarized.

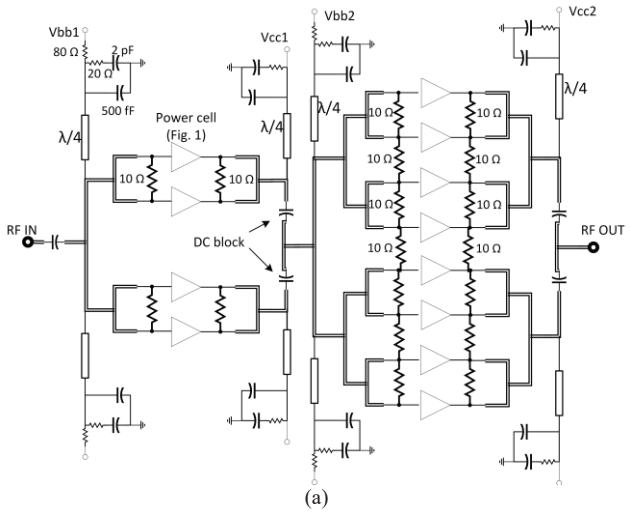
TABLE I. CIRCUIT PARAMETERS' VALUES

R_1	C_1	C_2	R_2	R_3
250 Ω	300 fF	80 fF	130 Ω	60 Ω

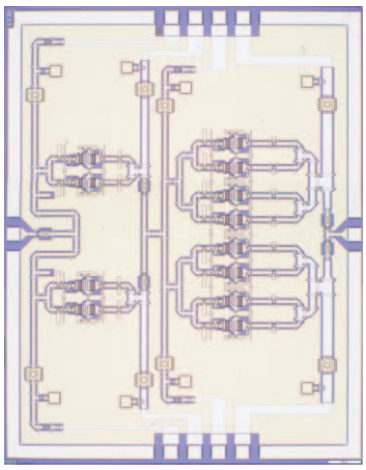
From the simulated small signal characteristics reported in Fig. 2, it can be seen that the power cell is unconditionally stable at all frequencies, with a maximum available gain (MAG) of 10 dB at 75 GHz. To evaluate its performance in large signal regime, it is useful to examine the dynamic load-line (Fig. 3a) and the time-domain voltage waveforms (Fig. 3b) taken at the collector nodes of Q_1 and Q_2 when the power cell is operating in saturation and with a load impedance Z_L=$Z_{opt,2}$=14+j8 Ω. The simulated voltage and current swings are within the safe operating area (SOA) and the output power is P_{sat}=18 dBm. There is a small phase misalignment between the two voltage waveforms v_{ce1} and v_{ce2} introduced by the finite interconnection L_{12}. This phase-shift, however, does not harm the reliability of the power cell, as the breakdown voltage is never exceeded.

B. MMIC Power Amplifier

The schematic representation of the two-stage InP DHBT power amplifier is shown in Fig. 4a. The power stage is composed of eight power cells combined in parallel by means of a corporate combiner implemented in CPW technology with characteristic impedance Z_0=50 Ω. The four-way combined driver stage has been implemented with the same principle. To suppress all odd-mode instabilities, 10-Ω resistors have been placed midway between adjacent power cells so the even mode is not affected. Bias networks are realized with quarter-wavelength stubs dynamically shorted by shunt capacitors. For dc decoupling and to suppress low frequency oscillations, RC series are placed close to the bias pads. A microphotograph of



(a)



(b)

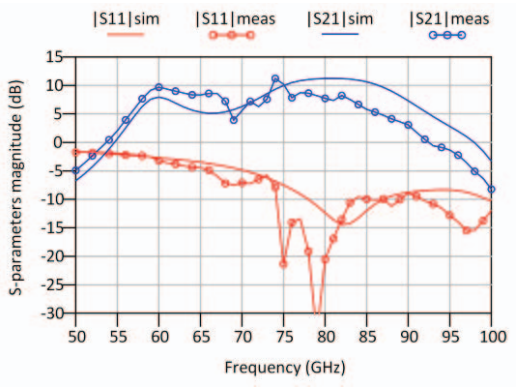
Fig. 4. Schematic representation (a) and chip microphotograph (b) of the two-stage InP DHBT power amplifier. The MMIC size is is 2.4×3.0 mm^2.

the InP DHBT power amplifier is shown in Fig. 4b. The MMIC size is 2.4×3.0 mm^2.

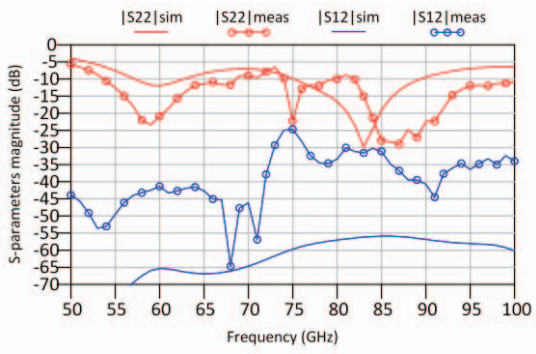
IV. Experimental Results

A. S-parameters

Power amplifier characterization has been carried out on wafer with RF GSG probes. S-parameters have been measured with an Anritsu VNA MS4647. In Fig. 5, measured S-parameters are compared with EM-circuit co-simulation results obtained on Keysight ADS. It can be seen that the measured data are slightly down-shifted in frequency with respect to simulations. The measured input return loss (Fig. 5a) is comparable with the simulated one and it is even higher between 75 GHz and 81 GHz, being better than 15 dB. The maximum measured gain is 11 dB at 74 GHz. The same value was obtained in simulation at 81 GHz. In Fig. 5b, the output return loss and the reverse isolation are shown. The latter is better than 25 dB at all frequencies.



(a)



(b)

Fig. 5 Simulated (solid line) and measured (solid line with symbols) S-parameters of the designed power amplifier.

B. Large signal measurements

The large signal behavior of the InP DHBT power amplifier has been measured at 75 GHz with a custom-made setup illustrated in Fig. 6. The sinusoidal signal source at 12.5 GHz is generated by the frequency synthesizer 68169B by Anritsu. The required 75-GHz signal is then obtained by means of the frequency multiplier (×6) RPG AFM6, which features a maximum output power of 7 dBm. A variable attenuator 0-50 dB is used for making the power sweep possible, and the medium power amplifier (MPA) RPG 7090 is used to restore acceptable levels of power fed into the device under test (DUT). The output power level is detected by the power sensor W8486A from Agilent and measured by the power meter Agilent N1914A. After calibration, it was found that the maximum power at the input probe-tips with this setup is 12.2 dBm, not enough to bring the power amplifier under test to saturation. The maximum measured output power, not corresponding to the saturated one, is 21.4 dBm and the 1-dB compression point is 18.6 dBm. The linear power gain is 12.6 dB, which seems optimistic if compared to S-parameter measurements. The small discrepancy could be attributed to the not perfectly calibrated homemade setup. The maximum PAE resulted in a quite low 3% due to the high DC current absorbed by the power amplifier and flowing to the resistive self-bias networks. In the small signal regime, the implemented power amplifier seems to exhibit better performances than the simulated one, but

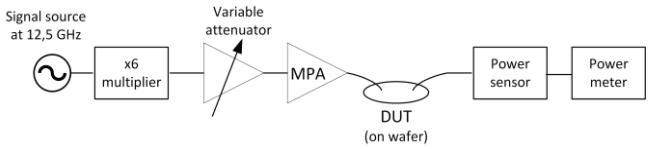


Fig. 6. Concept diagram of the large signal measurement setup at 75 GHz.

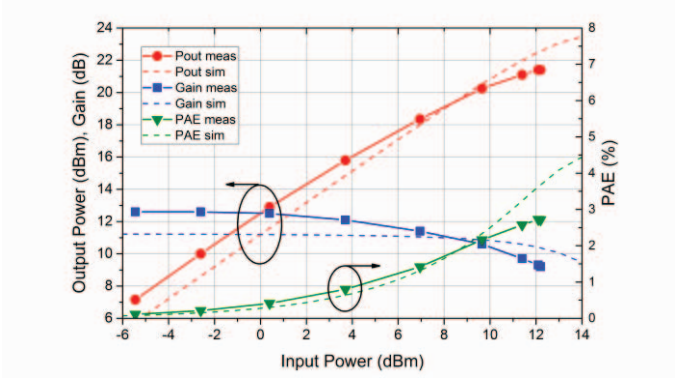


Fig. 7. Large signal characterization of the designed InP DHBT power amplifier at 75 GHz.

compression occurs earlier than predicted. Observing the output return loss in Fig. 5b, it can be inferred that, because of the frequency shift, the power amplifier is terminated with an output load slightly different from the optimum. This may be the reason for an early compression.

V. Conclusions

An InP DHBT power amplifier based on two-stacked transistors operating around 75 GHz has been designed and reported in this work. The operating principle of the basic power cell structure has been discussed. It has been optimized by EM-circuit co-simulations and its key performances have been highlighted. The power amplifier is made up of two stages: an eight-way combined power stage driven by a four-way combined driver stage. Power combination is realized with low loss corporate architectures implemented with CPW lines. Despite the fact that the transistors were optimized for high-speed mixed-signal applications, more than 21 dBm of output power and 12.6 dB of linear power gain have been obtained. Higher performances are expected from a power-optimized process currently underway. Moreover, a dedicated large signal measurement setup will allow the power amplifier to be fully saturated.

Acknowledgment

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References

[1] A. Scavennec, M. Sokolich, and Y. Baeyens, "Semiconductor Technologies for Higher Frequencies," *IEEE Microwave Magazine*, Vol. 10, Issue 2, pp. 77-87, April 2009.

[2] K. Datta and H. Hashemi, "High-Breakdown, High-f_{max} Multiport Stacked-Transistor Topologies for the W-band Power Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. 52, no. 5, pp. 1305-1319, May 2017.

[3] Y. Kim and Y. Kwon, "Analysis and Design of Millimeter-Wave Power Amplifier Using Stacked-FET Structure," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 2, pp. 691-702, February 2015.

[4] M. Gavell, I. Angelov, M. Ferndahl, and H. Zirath, "A High Voltage mm-Wave Stacked HEMT Power Amplifier in 0.1 µm InGaAs Technology," in *Proc. 2015 IEEE MTT-S International Microwave Symposium (IMS)*, 2015.

[5] P. Colantonio, F. Giannini, E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*, John Wiley & Sons, 2009.

[6] H.-F. Wu, Q.-F. Cheng, X.-G. Li, and H.-P. Fu, "Analysis and Design of an Ultrabroadband Stacked Power Amplifier in CMOS Technology," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, Vol. 63, no. 1, pp. 49-53, January 2016.

[7] J. Godin et al., "Submicron InP DHBT Technology for High-Speed High-Swing Mixed-Signal ICs," in *Proc. IEEE Compound Semiconductor Integrated Circuits Symposium (CSICS)*, October 2008.

[8] T. K. Johansen et al., "Large-Signal Modeling of Multi-finger InP DHBT Devices at Millimeter-Wave Frequencies", in *Proc. International Workshop on Integrated Nonlinear Microwave and Millimeter-Wave Circuits (INMMiC)*, April 2017.

[9] L. Yan and T. K. Johansen, "Design of InP DHBT Power Amplifiers at Millimeter-Wave Frequencies using Interstage Matched Cascode Technique," *Microelectronics Journal*, Vol. 44, Issue 12, pp. 1231-1237, September 2013.

[10] M. Squartecchia, T. K. Johansen, and V. Midili, "Design Procedure for Millimeter-Wave InP DHBT Stacked Power Amplifiers", in *Proc. International Workshop on Integrated Nonlinear Microwave and Millimeter-Wave Circuits (INMMiC)*, October 2015.

“Design Procedure for Millimeter-wave InP DHBT Stacked Power Amplifiers”

Design Procedure for Millimeter-wave InP DHBT Stacked Power Amplifiers

Michele Squartecchia[1], Tom K. Johansen[1], Virginio Midili[1]

[1]Department of Electrical Engineering, Technical University of Denmark, 2800 Lyngby, Denmark

Abstract — The stacked-transistor concept for power amplifiers (PA) has been investigated in this work. Specifically, this architecture has been applied in the design of millimeter-wave monolithic microwave integrated circuits (MMICs) using indium phosphide (InP) double heterojunction bipolar transistors (DHBTs). In this paper we describe the design methodology adopted and the results obtained at 86 GHz and 140 GHz. In the former case, 14.5 dBm of output power at the compression point, 14.5 dB of gain and 19.6 % of PAE are obtained from a four-transistor power cell. At 140 GHz, the same architecture gives 13.1 dBm of output power, 10.1 dB of gain and 13 % of PAE. To the best of the authors' knowledge, this is the first investigation of multi-level stacked PAs based on InP HBT technology.

Index Terms — Heterojunction bipolar transistor (HBT), Millimeter wave integrated circuits, MMIC, power amplifier, stacked transistors.

I. Introduction

Recently, wireless communications and radar applications are increasingly taking place at millimeter-wave bands. The aim behind this trend is to exploit the large bandwidths available at these frequencies. It is well known, however, that the main limitations of these systems are imposed by the power amplifier capabilities. In MMIC technology, one of the most challenging issues is the limited breakdown voltage of the transistors, which limits the output voltage swing. This aspect is becoming more and more critical with the continuous downscaling of devices.

To overcome the limited breakdown voltage, the series combination of transistors in stacked architectures is currently under investigation [1]-[4]. Stacking *n* devices, the overall output voltage swing can be *n* times larger than a single device and, as the current swing is the same, it results in an output power *n* times higher. Moreover, the optimum load impedance is increased by the same factor *n*, allowing the implementation of low-loss and broadband matching networks. In order to optimize the output power, the voltages across the devices must be of the same amplitude and phase-aligned. The latter condition is particularly challenging at millimeter-wave frequencies due to parasitic effects. This stacking concept has been widely investigated with FET transistors, but only a few works have been applied to bipolar transistors (e.g. [5]).

InP DHBT technology has proven attractive for its power handling capabilities at high millimeter-wave frequencies [6]. A millimeter-wave interstage matched Cascode configuration in InP DHBT was reported in [7]. In this work we investigate the possibility to implement multi-level stacked power amplifiers by using InP DHBTs at high millimeter-wave frequencies. We describe the procedure that can be followed in the design-flow of a stacked power-cell. This methodology has been adopted at two different frequencies (86 GHz and 140 GHz) and the corresponding results are compared.

II. Devices And Circuit Overview

In this work, InP DHBT single-finger devices are used to investigate the circuit topology. They are characterized by a collector-emitter breakdown voltage BV_{CE0}=4.9 V and f_T/f_{max}=330/420 GHz when biased at Vce=2.4 V and I_C=15 mA. In the design process, the non-linear UCSD HBT model is employed in circuit simulations.

In Fig. 1, the architecture of a four-transistor stacked power cell is shown. At the output of the common-emitter stage, a series of common-base stages is connected. The base terminals are connected to finite impedances through the capacitances C_k, so they are not tied to the ground voltage. This reduces the base-collector voltage swing and the relative breakdown is prevented. In order to maximize the performances of the circuit, each transistor should be matched

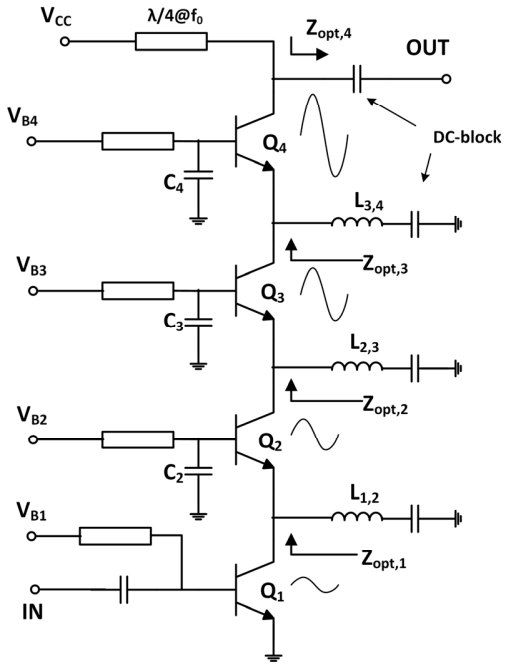

Fig. 1. Circuit schematic of a four-transistor stacked power cell.

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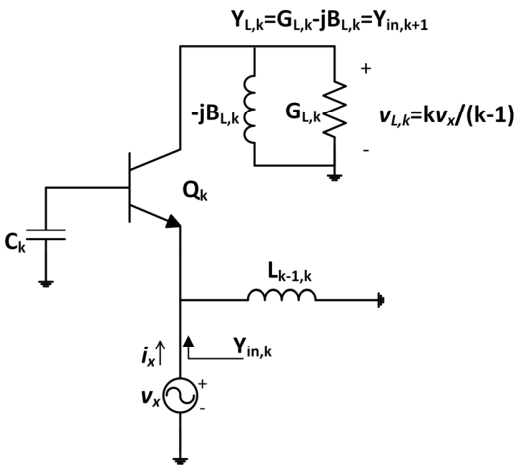

Fig. 2. Circuit schematic of the k-th stage of the power cell used to estimate C_k and $L_{k-1,k}$ (bias details omitted).

for maximum output power, and the corresponding optimum impedance $Z_{opt,k}$ should be connected to its output. For this purpose, shunt inductors $L_{k-1,k}$ are used as inter-stage matching between the transistors.

The amplitude of the overall output voltage is equally distributed among the devices. Moreover, for efficient power combining and for preventing collector-emitter breakdown, voltage phase-alignment is required. The following expression has to be satisfied:

$$v_{c,k} = \frac{k \cdot v_{c,k-1}}{k-1}, \qquad (1)$$

$v_{c,k}$ being the collector voltage of the k-th transistor.

All these requirements are accomplished by properly choosing the values of C_k and $L_{k-1,k}$ as described next.

III. Design Methodology

The first step in the design of the stacked power cell is to identify the optimum load of the common emitter-stage ($Z_{opt,1}$) through a load-pull simulation. The input impedance to the second stage, then, should be identical. In this regard, the circuit of Fig. 2 is used to evaluate $Y_{in,2}$, which is directly related to the values of C_2, $L_{1,2}$, and to the load admittance $Y_{L,2}$, which will coincide with the input admittance of the third stage. Due to the parasitic capacitances of the transistor, it is expected that the load susceptance must be negative.

In order to comply with (1), the first guess of the design is done by setting $G_{L,2} = 0.5\times\mathrm{Re}\{1/Z_{opt,1}\}$. In this condition, the values of C_2 and $B_{L,2}$ must be found in such a way to make v_x and $v_{L,2}$ phase-aligned and $\mathrm{Re}\{Y_{in,2}\}=\mathrm{Re}\{1/Z_{opt,1}\}$. At this point, v_x and $v_{L,2}$ are close to satisfy (1), but not exactly. In fact $v_{L,2} < 2\cdot v_x$ due to the intrinsic ohmic losses of the transistor that are taken into account in the model. For this reason, $G_{L,2}$ is slightly decreased and a new iteration is carried out. This procedure can be repeated a few times until

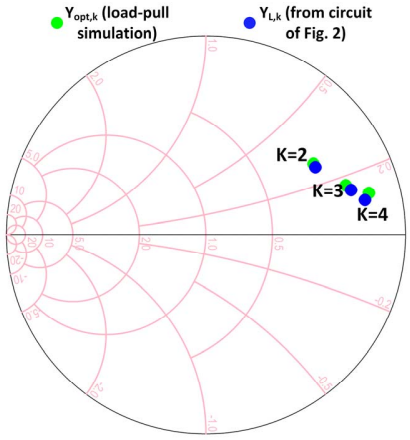

Fig. 3. Comparison between the admittances found by load-pull simulations (green) and the ones previously found (blue).

(1) is perfectly satisfied. The next step is to make $\mathrm{Im}\{Y_{in,2}\}=\mathrm{Im}\{1/Z_{opt,1}\}$ by properly tuning the value of $L_{1,2}$. At this point, a two-transistor power cell has been designed. If we perform a load-pull simulation on this power cell, it turns out that the optimum load admittance $1/Z_{opt,2}$ is close to $Y_{L,2}=G_{L,2}-jB_{L,2}$ just found, so the latter could be used as the starting point to design the third stage following the procedure just described.

In the Smith chart of Fig. 3, the optimum load admittances found in load-pull simulations for each stage are reported together with the admittances $Y_{L,k}$ found following our methodology. In some sense, their proximity is not surprising, as an admittance found from load-pull different from $Y_{L,k}$ would cause a mismatch between Q_k and Q_{k+1}, and hence a loss of power.

IV. Simulation Results

Following the design-flow described above, two four-transistor power cells have been implemented: one at 86 GHz

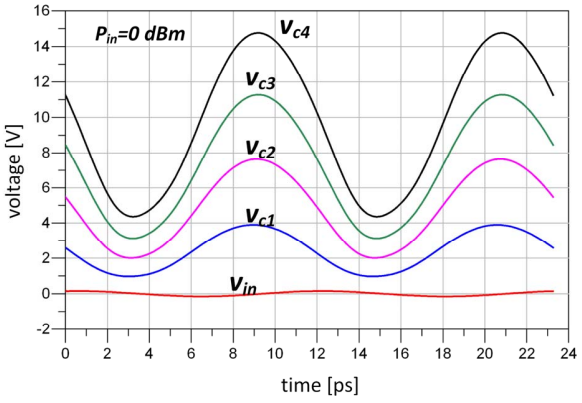

Fig. 4. Simulated voltage waveforms at each collector of the four-transistor stacked power cell at 86 GHz

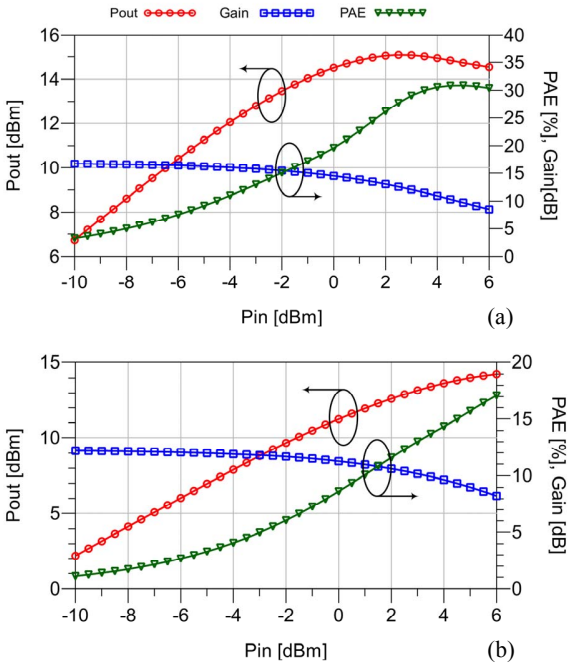

Fig. 5. Power sweep simulation of the four-transistor stacked power cells at 86 GHz (a) and at 140 GHz (b)

and one at 140 GHz, respectively. In Fig. 4, the voltage waveforms at each collector are depicted together with the input voltage waveform at 86 GHz. The input power has been set to P_{in}=0 dBm, which corresponds to the 1-dB compression point of the power cell designed at 86 GHz. It can be seen that the breakdown voltage of 4.9 V is never exceeded and (1) is satisfied in magnitude as well as in phase. This guarantees a high efficiency of the stacked power cell. A similar set of waveforms is obtained for the 140 GHz power cell and also in this case the condition (1) is satisfied.

Power sweep simulations have been carried out on the two power cells and the relative results are compared in Fig. 5. At the compression point, the power cell designed at 86 GHz exhibits an output power of 14.5 dBm, a gain of 14.5 dB and a power-added efficiency (PAE) of 19.6 %. For the power cell designed at 140 GHz, compression occurs with an input power equal to 3 dBm. At this point the output power is 13.1 dBm and the corresponding gain is 10.1 dB and PAE is 13 %.

It is clear that during the design flow of the four-transistor power cell, the intermediate steps are the design of the two- and three-transistor power cells. The output power of them has been monitored as well. In Fig. 6, the output power as a function of the number of transistors has been reported for both cases (86 GHz and 140 GHz). Taking the common-emitter stage as a reference (one-transistor), it can be seen that the total incremental output power is 5 dBm for the 86 GHz case and 4.5 dBm for the 140 GHz case.

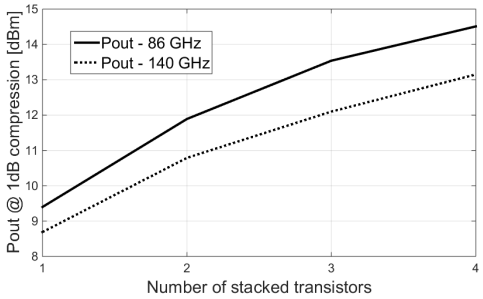

Fig. 6. Output power as a function of the number of stacked transistors

V. Conclusions

In this work we have investigated the possibility to apply the transistor-stacking concept to InP DHBT power amplifiers operating at high millimeter-wave frequencies. An effective design procedure has been described and applied to two different four-transistor stacked power cells operating at 86 GHz and 140 GHz, respectively. As expected, the performance is better at 86 GHz, however, the output power at 140 GHz is comparable and a driver amplifier could be used for compensating the lower gain. This work can pave the way for new millimeter-wave stacked power amplifier topologies still unexplored in InP technology.

VI. Acknowledgement

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References

[1] J. G. McRory, G. G. Rabjohn, R. H. Johnston, “Transformer Coupled Stacked FET Power Amplifiers,” *IEEE Journal of Solid-State Circuits,* vol. 34, no. 2, pp. 157-161, February 1999.

[2] S. Pornpromlikit, et al., “A Watt-Level Stacked-FET Linear Power Amplifier in Silicon-on-Insulator CMOS,” *IEEE Trans. Microwave Theory Techn.,* vol. 58, no. 1, pp. 57-64, January 2010.

[3] H. T. Dabag, et al., “Analysis and Design of Stacked-FET Millimeter-Wave Power Amplifiers,” *IEEE Trans. Microwave Theory Techn.,* vol. 61, no. 4, pp. 1543-1556, April 2013.

[4] Y. Kim, and Y. Kwon, “Analysis and Design of Millimeter-Wave Power Amplifier Using Stacked-FET Structure,” *IEEE Trans. Microwave Theory Techn.,* vol. 63, no. 2, pp. 691-702, February 2015.

[5] D. Fritsche, R. Wolf, F. Ellinger, “Analysis and Design of a Stacked Power Amplifier With Very High Bandwidth,” *IEEE Trans. Microwave Theory Techn.,* vol. 60, no. 10, pp. 3223-3231, October 2012.

[6] T. B. Reed, et. al., “A 180mW InP HBT Power Amplifier MMIC at 214 GHz,” *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)* - 2013.

[7] T. K. Johansen, et al., “Millimeter-wave InP DHBT Power Amplifier Based on Power-optimized Cascode Configuration,” *Microwave and Optical Technology Letters,* vol. 55, no. 5, May 2013.

“Design of a Planar Ultra-Wideband Four-Way Power Divider/Combiner Using Defected Ground Structures”

Design of a Planar Ultra-Wideband Four-Way Power Divider/Combiner Using Defected Ground Structures

Michele Squartecchia, Bruno Cimoli, Virginio Midili, Tom K. Johansen, Vitaliy Zhurbenko
Department of Electrical Engineering, Technical University of Denmark
2800 Kongens Lyngby, Denmark
micsqua@elektro.dtu.dk

***Abstract*—This work presents the design of a planar ultra-wideband (UWB) four-way power divider/combiner. A prototype has been fabricated on a printed circuit board and characterized. For achieving the frequency response required in UWB applications, each branch of the divider is conceived as a three-section Chebyshev impedance transformer. The defected ground structure (DGS) technique has been used to obtain the required high impedance lines. The power divider's insertion loss is 1 dB at 3.1 GHz and 2.9 dB at 10 GHz; the input reflection is lower than -10 dB, and the isolation between the output ports is better than 13 dB from 3 GHz to 10 GHz. A back-to-back configuration has been implemented as well. Its insertion loss is lower than 5 dB and its input reflection is lower than -10 dB over the UWB frequency range.**

***Keywords*—Power divider; ultra-wideband; defected ground structure.**

I. INTRODUCTION

Equiphase and equiamplitude *n*-way power combiners/dividers are essential components in many microwave systems, including power amplifiers, oscillators and antenna arrays. The Wilkinson power divider is perhaps the most popular due to its simple design and good performances in terms of losses, matching and isolation [1]. In the original formulation, the Wilkinson power divider utilizes a single quarter-wavelength impedance transformer section, which limits its fractional bandwidth. A wider bandwidth can be attained by means of a multiple-section divider, where each line is a stepped-impedance transformer designed for a maximally flat or equiripple response [2], [3]. The working principle, in either case (single- or multiple-section), relies on the electrical symmetry of the structure, allowing the isolation resistors to be connected to a central common node and suppress odd-mode propagations. For a planar implementation, known as fork power divider, perfect electrical symmetry is harder to obtain (unless n=2), and compensation techniques have to be adopted to make the external lines having the same electrical characteristics as the internal ones [4]. The corporate power combiner/divider, employing several 2-way Wilkinson, can offer an increased level of symmetry [5]-[7], but it is limited to cases where n is a power of two. Moreover, it may occupy a large area and exhibit relatively high losses [8], [9].

In this work, the design of a planar four-way three-section power combiner/divider suitable for ultra-wideband (UWB) applications is presented [10]. It provides a frequency range spanning from 3.1 GHz to 10.6 GHz and features a Chebyshev response. In such a design, lines with a high characteristic impedance are needed. Given a microstrip technology with a fixed substrate, the way to increase the characteristic impedance is to reduce the line width, eventually down to the limit of reliable manufacturability. To overcome this limit and obtain even higher values, the Defected Ground Structure (DGS) technique [11] has been exploited in this design. By lengthening the return path of the current, a higher value of the series inductance is obtained, so a line with high characteristic impedance has been realized and used as the first section of the Chebyshev power divider

In what follows, the circuit description and the design procedure of the divider are summarized. Its implementation and experimental results are reported. A back-to-back configuration is also presented with measurements results.

II. CIRCUIT DESIGN

A general schematic diagram of a three-section four-way power divider is shown in Fig. 1. A rigorous analysis should consider all possible excitation modes (one even-mode and three odd-modes in this case) and, by imposing a specific response in terms of reflection coefficients and isolation, should provide design formulas for calculating the characteristic impedances Z_k and the isolation resistances R_{kx} and R_{ki} (k=1,2,3) [12]. θ_k denotes the electrical length of the

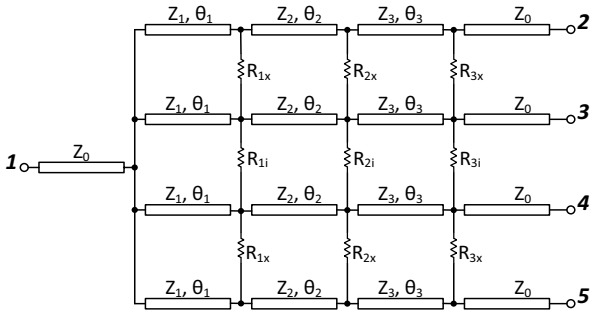

Fig. 1. Circuit schematic of a planar three-section four-way power combiner/divider

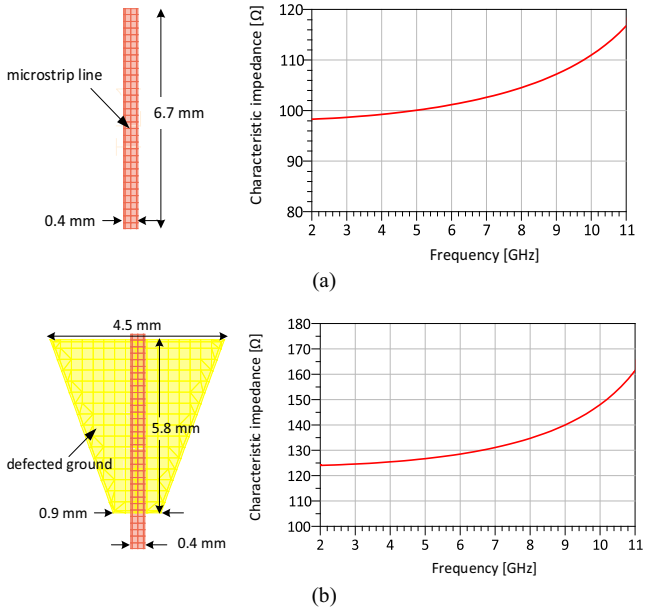

Fig. 2. EM-simulated characteristic impedance for a standard microstrip line (a) and for a microstrip with DGS structure (b) on Rogers RO4003C.

lines and should be equal to π/2 at the center frequency (7 GHz in our case). The design starts by considering the even-mode equivalent circuit, which consists of a three-section stepped-impedance line with characteristic impedances Z_k, transforming the Z_0 load up to $4Z_0$. In this design, it was decided to optimize the bandwidth and tolerate a small ripple, so the choice was to make the reflection coefficient having a Chebyshev response with a maximum value of -10 dB over the UWB frequency range. Considering the standard load termination Z_0=50 Ω and referring to the well-known tables available in the literature [2] led us to select Z_1=140 Ω, Z_2=100 Ω and Z_3=70 Ω. Isolation resistors can be found by imposing the suppression of all odd-modes. Exact theoretical formulas are given in [12] and in this case they give R_{1x}=R_{1i}=44 Ω, R_{2x}=R_{2i}=152 Ω and R_{3x}=R_{3i}=300 Ω. Because of the not perfect electrical symmetry, in real design R_{kx}≠R_{ki} resulted, and slightly different values were obtained after EM optimization. Moreover, the connections between the resistors introduce significant parasitic effects that harm the performances of the divider [13], and they have been taken into account and alleviated as much as possible.

III. Microstrip Implementation

A. Technology

The technology selected for this power divider is Rogers RO4003C, a 0.81 mm thick ceramic substrate with relative permittivity ε_r=3.55 and tanδ=0.0022 at 10 GHz, 35 µm thin copper layers on top and bottom. Resistors are implemented with S0402 SMD components. Keysight ADS has been used for circuit and EM simulations.

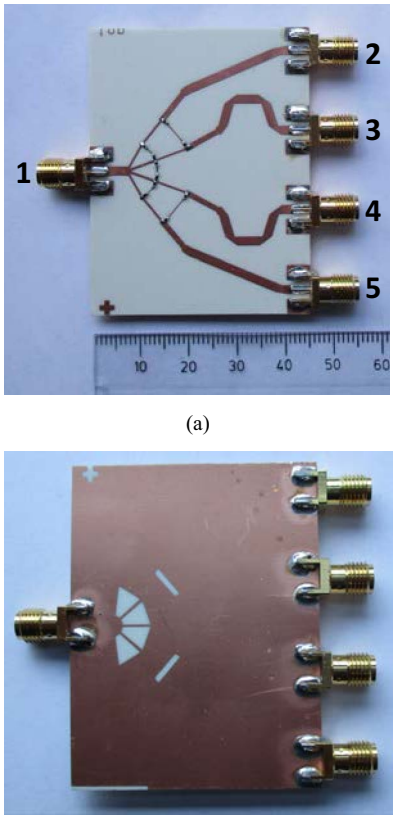

Fig. 3. Top (a) and bottom (b) views of the fabricated power divider/combiner

B. Defected Ground Structures

With the available fabrication tools, an acceptable accuracy is guaranteed for lines wider than 0.4 mm. In Fig. 2a, the layout of a 6.7 mm long (corresponding to a quarter-wavelength), 0.4 mm wide microstrip line is shown with its characteristic impedance obtained from EM simulations. In this technology, around 100 Ω has been obtained over the UWB frequency range, so it works for the second section of the impedance transformer. To obtain Z_1=140 Ω, a DGS has been drawn underneath a line of the same width (Fig. 2b). In light of the radial configuration of the full power divider, where all lines converge to the common input port, a trapezoidal shape has been selected for the DGS structure, whose dimensions have been established after an iterative optimization process. EM simulation results show a significant increase of the characteristic impedance. The DGS technique proved to be beneficial also when applied to the resistors' connections. Indeed, by lowering their parasitic capacitance to ground, it allows the frequency response of the divider to be unaffected.

C. Power Divider Layout

In Fig. 3a and 3b, the top view and the bottom view of the power divider are illustrated, respectively. Excluding the SMA connectors, it has a 44.9×57.8 mm^2 area. Having all output ports geometrically aligned, it is well suited for power amplifier applications, where it can be used as a combiner as well. A high combining efficiency is ensured by bending the central lines so that all ports have the same phase characteristics. EM simulations in ADS Momentum and iterative optimizations allowed us to select the optimum line widths and resistors' values, summarized in Table I. It was found that resistors R_{2i}, R_{3i} and R_{3x} do not improve isolation and matching significantly. Instead they introduce extra-losses, so they were eliminated from the design.

TABLE I. OPTIMIZED LINE WIDTHS AND RESISTOR VALUES

	k=1	*k=2*	*k=3*
Z_k	0.4 mm with DGS (140 Ω)	0.4 mm (100 Ω)	1.1 mm (70 Ω)
R_{kx}	86.6 Ω	340 Ω	*open*
R_{ki}	316 Ω	*open*	*open*

IV. MEASUREMENTS RESULTS AND DISCUSSION

Measurements have been carried out using the two-port VNA Hewlett Packard 8720D and compared with EM simulation results. In Fig. 4a, the insertion loss and the input reflection of the divider are reported. The reflection is well below -10 dB from 2.5 GHz to 11 GHz, even outperforming the UWB requirements, and it has the desired typical shape of a third order Chebyshev polynomial. In addition to the theoretical 6 dB, the insertion loss of the four-way power divider is 1 dB at 3.1 GHz and slightly increases at higher frequencies, reaching 2.9 dB at 10 GHz. Rather than being a design-related issue, it can be easily attributed to the relatively low-cost technology. Indeed, good agreement can be seen between simulations and measurements. In Fig. 4b, the output ports reflections are shown. Due to the adopted tradeoff between losses and matching in selecting the resistors, the output matching is not perfect, especially below 4 GHz, where the divider exhibits up to -6.5 dB of reflection at 3.1 GHz. At higher frequencies it behaves better, and only in a few frequency points the reflection is higher than -10 dB. Another issue that can be noted from these plots is the relative asymmetry: while internal ports 3 and 4 are practically identical, a small difference exists between the external ports 2 and 5. Again, this is due to fabrication uncertainties rather than design issues. Isolation between the output ports is reported in Fig. 4c. The best isolation performances are seen between ports 3 and 4, being better than 15 dB over the whole UWB range. Only slightly worse, 14 dB, is the isolation between ports 2 and 4. In all other cases, 13 dB, at worst, is observed.

The electrical symmetry of the proposed power divider can

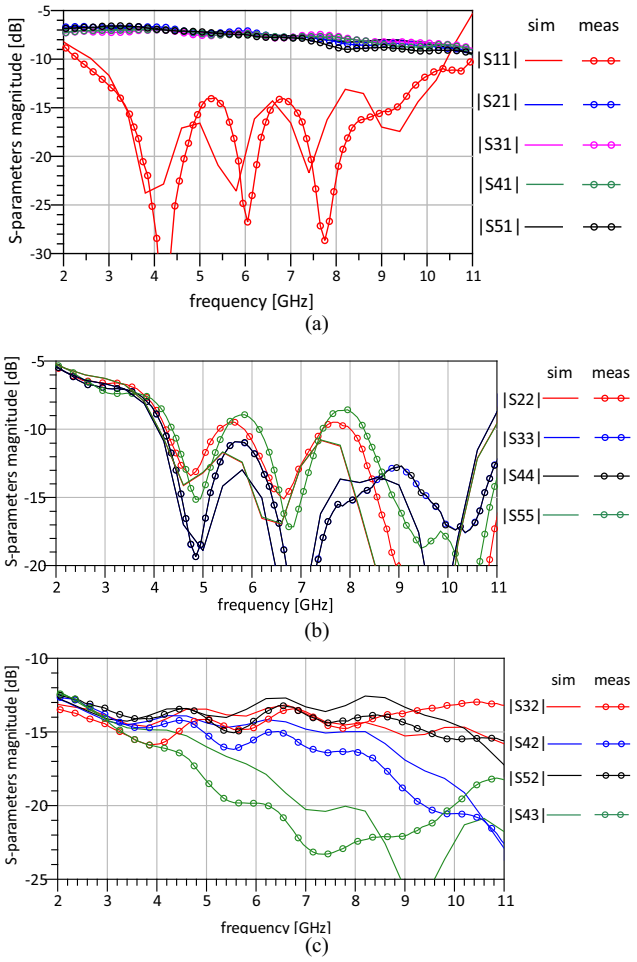

Fig. 4. Simulated and measured responses of the power divider: input reflection and insertion loss (a); ouput reflections (b); isolation between the output ports (c).

be further analyzed by looking at Fig. 5a and Fig. 5b, where the measured amplitude imbalance and phase imbalance are reported, respectively, and compared with simulations. The highest amplitude imbalance exhibited by the power divider is 0.6 dB in absolute value. Performance degradation is more significant only above 7 GHz. While the amplitude imbalance between ports 2 and 3 can be attributed to the different electrical characteristics between the lines (straight and bended for instance), the imbalance between ports 2 and 5, which should be perfectly symmetric, can only be due to fabrication and/or resistors' uncertainties. Regarding the phase imbalance reported in Fig. 5b, it can be seen that it is only 4º under 8 GHz between all ports. At higher frequencies, the phase imbalance reaches 6º between ports 2 and 4, and 8º between ports 2 and 5.

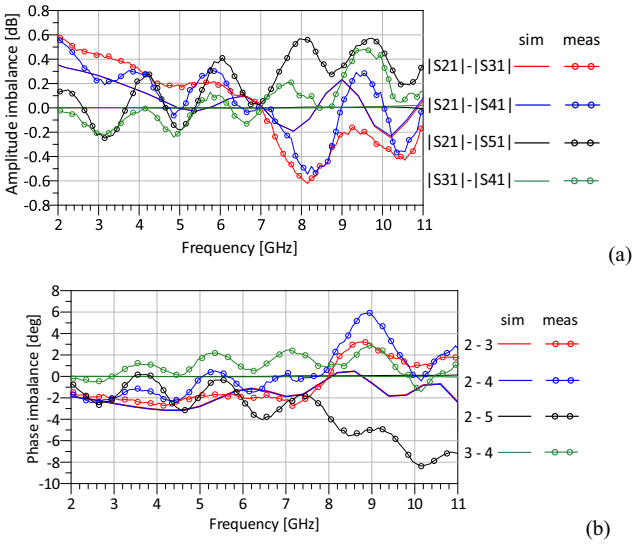

Fig. 5. Simulated and measured amplitude imbalance (a) and phase imbalance (b) of the power divider.

V. Back-to-Back Configuration

In power amplifier design, it is common practice to employ several power devices in parallel in order to achieve higher RF transmitting power, so a power divider is needed to split the input signal. Unless the amplified signals are fed to a transmitting antenna array, they need to be recombined. This is often done by reversing a copy of the divider. To account of all the losses taking place in the passive circuits of the power amplifier, the performances of a back-to-back structure have been investigated. In Fig. 6a, the back-to-back configuration of our power divider/combiner is shown, and in Fig. 6b, its measured frequency response is reported and compared with simulations. Besides the good agreement between the two, it can be seen that the insertion loss is lower than 2 dB at 3 GHz, but increases at higher frequencies, reaching 5 dB at 10 GHz. Reflections are lower than -10 dB.

VI. Conclusions

In this work, an ultra-wideband planar four-way power divider/combiner with a Chebyshev response, suitable for power amplifiers, has been designed and investigated. The defected ground structure technique has been used to realize the high impedance lines. Some tradeoffs in the choice of the isolation resistors and a relatively low-cost technology are responsible for moderate losses at high frequencies. Very good agreement between measurements and simulations has been observed. Prospective works could include implementations of the same concept on other technologies and/or higher frequencies of operation, eventually millimeter-waves.

Acknowledgment

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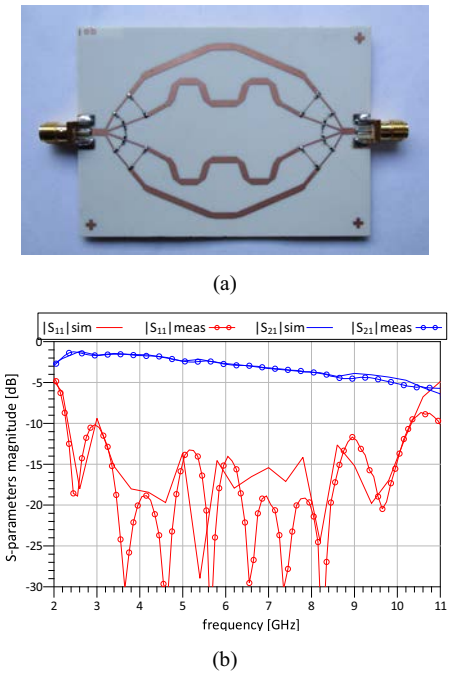

Fig. 6. Back-to-back power divider top view (a) and S-parameters (b).

References

[1] E. J. Wilkinson, "An N-Way Hybrid Power Divider," *IRE Trans. on Microwave Theory and Techniques*, vol. 8, pp 116-118, January 1960.

[2] D. M. Pozar, *Microwave Engineering,* 4th edition, John Wiley & Sons, 2012.

[3] H. Y. Yee, F.-C. Chang, N. F. Audeh, "N-Way TEM-Mode Broad-Band Power Dividers," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-18, no. 10, pp 682-688, October 1970.

[4] A. A. M. Saleh, "Planar Electrically Symmetric *n*-Way Hybrid Power Dividers/Combiners," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-28, no. 6, pp 555-563, June 1980.

[5] P. Colantonio, F. Giannini, E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*, John Wiley & Sons, 2009.

[6] T. Zhang, W. Che, H. Chen, W. Feng, "A Compact Four-Way Dual-Band Power Divider Using Lumped Elements," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 2, pp 94-96, February 2015.

[7] V. Zhurbenko, T. Rubæk, V. Krozer, P. Meincke, "Design and Realisation of a Microwave Three-dimensional Imaging System with Application to Breast-cancer Detection," *IET Microwaves, Antennas and Propagations*, Vol. 4, Issue 12, pp 2200-2211, December 2010.

[8] Z. Galani, S. J. Temple, "A Broadband Planar N-Way Combiner/Divider," *1977 IEEE MTT-S International Microwave Symposium Digest*, pp. 499-502, June 1977.

[9] T.-H. Tseng, Y.-S. Lin, "Miniature Broadband Four-Way Power Divider in Glass-Based Thin-Film Integrated Passive Device Technology," *2013 IEEE MTT-S International Microwave Symposium Digest*, 2013.

[10] I. Oppermann, M. Hämäläinen, J. Iinatti, *UWB Theory and Applications*, John Wiley & Sons, 2004.

[11] R. Garg, I. Bahl, M. Bozzi, *Microstrip Lines and Slotlines*, 3rd edition, Artech House, 2013.

[12] N. Nagai, E. Maekawa, K. Ono, "New *n*-Way Hybrid Power Dividers," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-25, no. 12, pp 1008-1012, December 1977.

[13] S. Horst, R. Bairavasubramanian, M. M. Tentzeris, J. Papapolymerou, "Modified Wilkinson Power Dividers for Millimeter-Wave Integrated Circuits," *IEEE Trans. on Microwave Theory and Techniques*, vol. 55, no. 11, pp 2439-2446, November 2007.

Bibliography

[1] K. C. Huang and Z. Wang, *Millimeter-Wave Communication Systems*, John Wiley Sons, Inc., Hoboken, New Jersey, 2011.

[2] G. E. Weibel and H. O. Dressel, "Propagation Studies in Millimeter-Wave Link Systems," *Proceedings of the IEEE*, Vol. 55, no. 4, pp. 497-513, April 1967.

[3] J. Wells, "Faster Than Fiber: The Future of Multi-Gb/s Wireless," *IEEE Microwave Magazine*, vol. 10, Issue 2, pp. 77-87, April 2009.

[4] N. Kukutsu, et al., "Toward practical applications over 100 GHz," *IEEE MTT-S International Microwave Symposium Digest*, 2010.

[5] A. G. Pakhomov and M. R. Murphy, "Low-intensity Millimeter Waves as a Novel Therapeutic Modality," *IEEE Transactions on Plasma Science*, Vol. 28, no. 1, pp. 34-40, January 2000.

[6] Z. Pi and F. Khan "An Introduction to Millimeter-Wave Mobile Broadband Systems," *IEEE Communications Magazine*, Vol. 49, Issue 6, pp. 101-107, June 2011.

[7] S. Chia, M. Gasparroni, and P. Brick, "The Next Challenge for Cellular Networks: Backhaul," *IEEE Microwave Magazine*, Vol. 10, Issue 5, pp. 54-66, August 2009.

[8] P. Harati, et al., "Is E-Band Satellite Communication Viable?," *IEEE Microwave Magazine*, vol. 18, Issue 7, pp. 64-76, November 2017.

[9] "Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2016–2021," Available online: www.cisco.com/c/en/us/solutions/service-provider/visual-networking-index-vni/index.html, 2017.

[10] F. Boes, et al., "Multi-Gigabit E-band Wireless Data Transmission," *IEEE MTT-S International Microwave Symposium Digest*, 2015.

[11] D. Zhao and P. Reynaert, *CMOS 60-GHz and E-band Power Amplifiers and Transmitters*, Springer International Publishing Switzerland, 2015.

[12] J. L. B. Walker, *Handbook of RF and Microwave Power Amplifiers*, Cambridge University Press, 2012.

[13] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, 2006.

[14] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *IRE International Convention Record*, vol. 13, pp. 27-34, 1965.

[15] P. Colantonio, F. Giannini, and E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*, John Wiley & Sons Ltd, 2009.

[16] L. Yan, T. K. Johansen, and J. Kammersgaard, "Stability Investigation for InP DHBT mm-Wave Power Amplifier," *International Journal of RF and Microwave Computer-Aided Engineering*, Vol. 23, Issue 6, pp. 662-674, October 2013.

[17] X. Mei, et al., "First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process," *IEEE Electron Device Letters*, Vol. 36, no 4, pp. 327-329, April 2015.

[18] A. Scavennec, M. Sokolich, and Y. Baeyens, "Semiconductor Technologies for Higher Frequencies," *IEEE Microwave Magazine*, vol. 10, Issue 2, pp. 77-87, Apr. 2009.

[19] S. Voinigenscu, *High-Frequency Integrated Circuits*, Cambridge University Press, 2013.

[20] A. Bessemoulin, J. Tarazi, M. Rodriguez, M. G. McCulloch, A. E. Parker, and S. J. Mahon, "Reduced-size E-band GaAs Power Amplifier MMIC," *Proceedings of the* 10^{th} *European Microwave Integrated Circuits Conference (EuMIC)*, September 2015.

[21] A. Bessemoulin, M. Rodriguez, J. Tarazi, M. G. McCulloch, A. E. Parker, and S. J. Mahon, "Compact W-band PA MMICs in Commercially Available 0.1-µm GaAs PHEMT Process," *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2015.

[22] K. Datta and H. Hashemi, "A 29dBm 18.5% Peak PAE mm-Wave Digital Power Amplifier with Dynamic Load Modulation," *2015 IEEE International Solid-State Circuits Conference*, February 2015.

[23] K. Datta and H. Hashemi, "High-Breakdown, High-$f_{\max}$ Multiport Stacked-Transistor Topologies for the W-Band Power Amplifier," *IEEE Journal of Solid-State Circuits*, Vol. 52, no. 5, pp. 1305-1319, May 2017.

[24] J. F. Buckwalter, S. Daneshgar, J. Jayamon, and P. Asbeck, "Series Power Combining: Enabling Techniques for Si/SiGe Millimeter-wave Power Amplifiers," *2016 IEEE* 16^{th} *Topical Meeting on Silicon Monolithic Integrated Circuits in Rf Systems*, 2016.

[25] Y.-H. Hsiao, Z.-M. Tsai, H.-C. Liao, J.-C. Kao, and H. Wang, "Millimeter-Wave CMOS Power Amplifiers With High Output Power and Wideband Performances," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 61, no 12, pp. 4520-4533, December 2013.

[26] A. Agah, J. A. Jayamon, P. M. Asbeck, L. E. Larson, and J. F. Buckwalter, "Multi-Drive Stacked-FET Power Amplifiers at 90 GHz in 45 nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 49, no 5, pp. 1148-1157, May 2014.

[27] D. Zhao and P. Reynaert, "An E-Band Power Amplifier With Broadband Parallel-Series Power Combiner in 40-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 63, no 2, pp. 683-690, February 2015.

[28] A. Brown, et al., "High Power, High Efficiency E-Band GaN Amplifier MMICs," *2012 IEEE International Conference on Wireless Information Technology and Systems (ICWITS)*, 2012.

[29] M. Micovic, et al., "92-96 GHz GaN power amplifiers," *2012 IEEE MTT-S International Microwave Symposium (IMS)*, 2012.

[30] M. Urteaga, Z. Griffith, M. Seo, J. Hacker, and M. J. W. Rodwell, "InP HBT Technologies for THz Integrated Circuits," *Proceedings of the IEEE*, Vol. 105, no 6, pp. 1051-1067, June 2017.

[31] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "340-440mW Broadband, High-Efficiency E-band PA's in InP HBT," *2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2015.

[32] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "190-260GHz High-Power, Broadband PA's in 250nm InP HBT," *2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2015.

[33] T. B. Reed, Z. Griffith, P. Rowell, M. Field, and M. Rodwell, "A 180mW InP HBT Power Amplifier MMIC at 214 GHz," *2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2013.

[34] H. G. Yu, S. H. Choi, S. Jeon, and M. Kim, "300 GHz InP HBT amplifier with 10 mW output power," *Electronics Letters*, vol. 50, no. 5, pp. 377-379, February 2014.

[35] J. Hacker, M. Urteaga, M. Seo, A. Skalare, and R. Lin, "InP HBT Amplifier MMICs Operating to 0.67 THz," *2013 IEEE MTT-S International Microwave Symposium (IMS)*, 2013.

[36] T. Al-Sawaf, K. Nosaeva, N. G. Weimann, V. Krozer, and W. Heinrich, "A 200 mW InP DHBT W-band Power Amplifier in Transferred-Substrate Technology with Integrated Diamond Heat Spreader," *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016.

[37] V. Radisic, et al., "Power Amplification at 0.65 THz Using InP HEMTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 3, pp. 724-729, March 2012.

[38] K. Leong, et al., "Progress in InP HEMT Submillimeter Wave Circuits and Packaging," *2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2015.

[39] M. Golio, *RF and Microwave Semiconductor Device Handbook*, CRC Press, 2003.

[40] H. Kroemer, "Theory of a wide-gap emitter for transistors," *Proc. IRE*, vol. 45, no. 11, pp. 1535-1537, November 1957.

[41] H. Kroemer, "Heterostructure Bipolar Transistors and Integrated Circuits," *Proc. IEEE*, vol. 70, no. 1, pp. 13-25, January 1982.

[42] M. J. W. Rodwell, et al., "Submicron Scaling of HBTs," *IEEE Transactions on Electron Devices*, vol. 48, no. 11, pp. 2606-2624, November 2001.

[43] N. Kashio, K. Kurishima, M. Ida, and H. Matsuzaki, "InP/InGaAs double heterojunction bipolar transistors with $BV_{\mathrm{CEO}} = 12$ V and $f_{\max} = 470$ GHz," *Electronics Letters*, vol. 51, no. 8, pp. 648-649, April 2015.

[44] R. Flückiger, R. Lövblom, M. Alexandrova, O. Ostinelli, and C. R. Bolognesi, "Type-II InP/GaAsSb double-heterojunction bipolar transistors with $f_{\max}$ >700 GHz," *Applied Physics Express*, vol. 7, Issue 3, March 2014.

[45] J. Godin, et al., "Submicron InP DHBT Technology for High-Speed High-Swing Mixed-Signal ICs," in *Proc. IEEE Compound Semiconductor Integrated Circuits Symposium (CSICS)*, October 2008.

[46] V. Nodjiadjim, et al., "400 GHz F_{MAX} InP/GaAsSb HBT for Millimeters-Wave Applications," in *Proc. International Conference on Indium Phosphide and Related Materials (IPRM)*, 2010.

[47] V. Midili, et al., "InP DHBT technology for power amplifiers at mm-wave frequencies," *Microelectronics Journal*, vol. 67, pp. 111-119, August 2017.

[48] T. K. Johansen, V. Nodjiadjim, and A. Konczykowska, "PAssive and electro-optic polymer photonics and InP electronics iNtegration for multi-flow Terabit transceivers at edge SDN switcHes and data-centER gateways," Technical Deliverable, August 2015.

[49] T. K. Johansen, et al., "Large-Signal Modeling of Multi-finger InP DHBT Devices at Millimeter-Wave Frequencies," in *Proc. International Workshop on Integrated Nonlinear Microwave and Millimeter-Wave Circuits (INMMiC)*, April 2017.

[50] J. McMacken, S. Nedeljkovic, J. Gering, and D. Halchin, "HBT Modeling," *IEEE Microwave Magazine*, vol. 9, Issue 2, pp. 48-72, April 2008.

[51] T. K. Johansen, R. Leblanc, J. Poulain, and V. Delmouly, "Direct Extraction of InP/GaAsSb/InP DHBT Equivalent-Circuit Elements From *S*-Parameters Measured at Cut-Off and Normal Bias Conditions," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 1, pp. 115-124, Jan. 2016.

[52] W. Liu, H-F. Chau, and E. Beam, "Thermal Properties and Thermal Instabilities of InP-Based Heterojunction Bipolar Transistors," *IEEE Transactions on Electron Devices*, vol. 43, no. 3, pp. 388-395, March 1996.

[53] V. Midili, M. Squartecchia, T. K. Johansen, V. Nodjiadjim, M. Riet, J.-Y. Dupuy, and A. Konczykowska, “A Physical Based Equivalent Circuit Modeling Approach for Ballasted InP DHBT Multi-Finger Devices at Millimeter-Wave Frequencies,” in *28^{th} International Conference on Indium Phosphide and Related Materials (IPRM)*, June 2016.

[54] G. Gao, M. S. Ünlü, H. Morkog, and D. L. Blackbum, “Emitter Ballasting Resistor Design for, and Current Handling Capability of AlGaAs/GaAs Power Heterojunction Bipolar Transistors,” *IEEE Transactions on Electron Devices*, vol. 38, no. 2, pp. 185-196, February 1991.

[55] R. Mezui-Mintsa, N. Hassaïne, M. Riet, B. Villeforceix, A. Konczykowska, S. Vuye, and H. Wang, “Accurate Analysis of Emitter Ballasting in HBT Power Transistors,” *Microelectronic Engineering*, vol. 19, pp. 777-780, 1992.

[56] C. Svensson, and G. E. Dermer, “Time Domain Modeling of Lossy Interconnects,” *IEEE Transactions on Advanced Packaging*, vol. 24, no. 2, pp. 191-196, May 2001.

[57] A. R. Djordjević, R. M. Biljić, V. D. Likar-Smiljanić, and T. K. Sarkar, “Wideband Frequency-Domain Characterization of FR-4 and Time-Domain Causality,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 4, pp. 662-667, November 2001.

[58] T. Johansen, C. Jiang, D. Hadziabdic, V. Krozer, “EM Simulation Accuracy Enhancement for Broadband Modeling of On-Wafer Passive Components,” in *Proc. European Microwave Conference (EuMC)*, October 2007.

[59] M. Shifrin, Y. Ayasli, and P. Katzin, “A New Power Amplifier Topology with Series Biasing and Power Combining of Transistors," *IEEE Microwave and Millimeter-wave Monolithic Circuits Symposium Digest*, pp. 39-41, 1992.

[60] J. Jeong, S. Pornpromlikit, P. M. Asbeck, and D. Kelly, “A 20 dBm Linear RF Power Amplifier Using Stacked Silicon-on-Sapphire MOSFETs," *IEEE Microwave and Wireless Components Letters*, Vol. 16, no. 12, pp. 684-686, Dec. 2006.

[61] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, “A Watt-Level Stacked-FET Linear Power Amplifier in Silicon-on-Insulator CMOS," *IEEE Trans. Microw. Theory Techn.*, Vol. 58, no. 1, pp. 57-64, Jan. 2010.

[62] C. Lee, et al., “A 18 GHz Broadband Stacked FET Power Amplifier Using 130 nm Metamorphic HEMTs," *IEEE Microwave and Wireless Components Letters*, Vol. 19, no. 12, pp. 323-325, Dec. 2009.

[63] D. Fritsche, R. Wolf, and F. Ellinger, “Analysis and Design of a Stacked Power Amplifier with Very High Bandwidth," *IEEE Trans. Microw. Theory Techn.*, Vol. 60, no. 10, pp. 3223-3231, Oct. 2012.

[64] A. K. Ezzeddine, H. C. Huang, and J. L. Singer, “UHiFET – A New High-Frequency High-Voltage Device," *IEEE MTT-S International Microwave Symposium*, 2011.

[65] H.-F. Wu, Q.-F. Cheng, X.-G. Li, and H.-P. Fu, “Analysis and Design of an Ultrabroadband Stacked Power Amplifier in CMOS Technology," *IEEE Trans. Circuits and systems II: Express Briefs*, vol. 3., no. 1, pp. 49-53, Jan. 2016.

[66] A. Agah, H. Dabag, B. Hanafi, P. Asbeck, L. Larson, J. Buckwalter “A 34% PAE, 18.6dBm 42-45GHz Stacked Power Amplifier in 45nm SOI CMOS," *IEEE Radio Frequency Integrated Circuits Symposium Digest*, 2012.

[67] H.-T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, “Analysis and Design of Stacked-FET Millimeter-Wave Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, Vol. 61, no. 4, pp. 1543-1556, Apr. 2013.

[68] A. Agah, J. A. Jayamon, P. M. Asbeck, L. E. Larson, and J. F. Buckwalter, “Multi-Drive Stacked-FET Power Amplifiers at 90 GHz in 45 nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 49, no. 5, pp. 1148-1157, May 2014.

[69] A. Chakrabarti and H. Krishnaswamy, “High-Power High-Efficiency Class-E-Like Stacked mmWave PAs in SOI and Bulk CMOS: Theory and Implementation," *IEEE Trans. Microw. Theory Techn.*, Vol. 62, no. 8, pp. 1686-1704, Aug. 2014.

[70] Y. Kim and Y. Kwon, “Analysis and Design of Millimeter-Wave Power Amplifier Using Stacked-FET Structure," *IEEE Trans. Microw. Theory Techn.*, Vol. 63, no. 2, pp. 691-702, Feb. 2015.

[71] M. Gavell, I. Angelov, M. Ferndahl, and H. Zirath, “A High Voltage mm-wave Stacked HEMT Power Amplifier in 0.1 μm InGaAs Technology," *IEEE MTT-S International Microwave Symposium*, 2015.

[72] T. K. Johansen, L. Yan, J.-Y. Dupuy, V. Nodjiadjim, A. Konczykowska, and M. Riet, “Millimeter-Wave InP DHBT Power Amplifier Based on Power-Optimized Cascode Configuration," *Microwave and Optical Technology Letters*, Vol. 55, no. 5, pp. 1178-1182, May 2013.

[73] L. Yan and T. K. Johansen, “Design of InP DHBT power amplifiers at millimeter-wave frequencies using interstage matched cascode technique," *Microelectronics Journal*, vol. 44, no. 12, pp. 1231-1237, Sep. 2013.

[74] M. Squartecchia, et al., “75 GHz InP DHBT Power Amplifier Based on Two-Stacked Transistors," *Proc. Asia Pacific Microwave Conference (APMC)*, 2017.

[75] J. E. Green, R. C. Tozer, and J. P. R. David, “Stability in Small Signal Common Base Amplifiers," in *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 60, no. 4, pp. 846-855, Apr. 2013.

[76] S. Dellier, R. Gourseyrol, J.-M. Collantes, and A. Anakabe, “Stability Analysis of Microwave Circuits,” *Wireless and Microwave Technology Conference*, 2012.

[77] A. Anakabe, N. Ayllón, J.M. Collantes, A. Mallet, G. Soubercaze-Pun, K. Narendra, "Automatic Pole-Zero Identification for Multivariable Large-Signal Stability Analysis of RF and Microwave Circuits," *European Microwave Conference (EuMC)*, 2010.

[78] D. M. Pozar, *Microwave Engineering*, Fourth Edition, John Wiley & Sons, Inc., 2012.